D 2390 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2009

EE 04-503—PULSE AND DIGITAL ELECTRONICS

(2004 admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

1. (a) Explain Current Sweep generation with a neat diagram.
   (b) Explain the Switching Behaviour of transistors.
   (c) Explain half-subtractor with a logic diagram.
   (d) Explain Decoder with a neat diagram.
   (e) Explain D flip-flop with its symbol and truth table.
   (f) Explain Ring-Counter with a neat diagram.
   (g) Explain about the flags in 8085 processor.
   (h) Explain programme counter with a neat diagram.

   (8 × 5 = 40 marks)

2. (a) (i) Write short notes on voltage sweep errors with a neat diagram. (7 marks)
   (ii) Explain Schottky BJT with a neat diagram. (8 marks)

   Or

   (b) Explain collector coupled monostable Schmitt Trigger Circuit with a neat diagram. (15 marks)

3. (a) (i) Minimize the expression :

$$Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}.$$

   (8 marks)

   (ii) Implement the following Boolean function using 8 : 1 MUX :

$$F(P, Q, R, S) = \Sigma m\ (0, 1, 3, 4, 8, 9, 15).$$

   (7 marks)

   Or

   (b) (i) What is ROM ? Explain the various types of ROM. (7 marks)
   (ii) Design full adder using two half-adder. (8 marks)

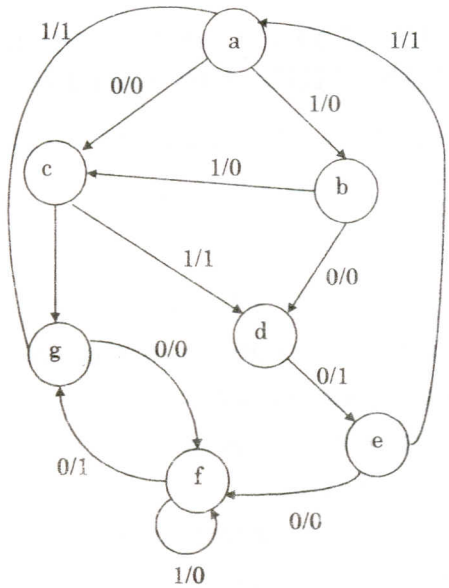
4. (a) (i) Explain synchronous counters with a neat diagram. (8 marks)
   (ii) Write short notes on ASM charts. (7 marks)

   Or

[redacted]

Turn over

(b) Draw state table for the state diagram shown in figure.



(15 marks)

5. (a) Explain data-bus, control bus and address bus with a neat diagram.

Or

(b) Explain the Architecture of 8085 with a neat diagram.

(15 marks)

[4 × 15 = 60 marks]