Roll No .....

EI - 701

B.E. VII Semester

Examination, December 2015

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.
iv) Except numericals, Derivation, Design and Drawing etc.

1. a) What are different operating regions of an MOS transistor?
   b) What is channel length modulation?
   c) For an NMOS transistor for which $V_{Tn} = 0.8V$, operating with V_{GS} in the range of 1.5 V to 4V, what is the range of V_{DS} for which channel remains in linear region?
   d) Derive the drain current equation for an N-Channel Mosfet.

OR

Explain the second order effects with their equations.

2. a) What are the advantages of CMOS inverter over the other configurations?
   b) In CMOS technology, why do we design the size of PMOS to be higher than the NMOS?
   c) Compare between CMOS and Bipolar technologies.
   d) Give the CMOS inverter DC transfer characteristics and operating regions.

OR

Consider a CMOS inverter circuit with the following parameters: $V_{DD} = 3.3V$, $V_{To,n} = 0.6V$, $V_{To,p} = -0.7$ V, $Kn = 200\ \mu A/V^2$, $Kp = 80\ \mu A/V^2$. Calculate the noise margins for the above circuit.

3. a) What are the various CMOS Technologies?
   b) What is twin tub process? Why it is so called?
   c) What is meant by interconnect? What are types of interconnect ?
   d) What are the lay-out design rules? Explain in details.

OR

Explain the latch - up prevention techniques.

4. a) What are the issues to be considered for circuit characterization and performance estimation?
   b) Explain the Rise time, Fall time and delay time.
   c) For a CMOS inverter assume, C= 150 fF and $V_{DD} = 5V$. The inverter is cycled through the low and high voltage levels at an average rate of f = 75 MHZ. Calculate the dynamic power dissipation.
   d) What are two components of power dissipation in CMOS inverter? Explain in details.

OR

Briefly explain about the CMOS transistor sizing.

5. a) What are the types of programmable devices?
   b) What are the various VLSI design style?
   c) Give the features of VHDL.
   d) Draw the block diagram of an FPGA and give its characteristics.

OR

Describe the steps in ASIC design flow.

******