S.F. ETRx III (Rw)
Digital System Design I

RK-1242

(3 Hours)　　　　　　[Total Marks : 100

N.B. : Question No. 1 is compulsory. Solve any four from rest six.

1.　Answer the following questions: Each question carries 5 marks.　　　20

　　(a) Construct Hamming code for BCD 0111. Use even parity.

　　(b) Construct an EX-OR gate using universal gates.

　　(c) Draw the circuit of 2-input TTL NAND gate.

　　(d) Explain with example self-complementing codes

2.　(a) Simplify the following 4 variable Boolean expression using Quine-　　10
　　McCluskey method
　　$F = \Sigma m\,(0,1,3,7,9,15) + d(8,11)$

　　(b) For the expression $Y = (P + Q)(Q'+R')$

　　　　i) Convert to standard POS　　　　　　　　　　　　　　4

　　　　ii) Reduce using K-map　　　　　　　　　　　　　　　4

　　　　iii) Construct circuit using NOR gates only　　　　　　　2

3.　(a) Implement the following expression using IC 74138, 3:8 active low decoder
　　　and additional gates
　　　$F(A,B,C,D) = \pi M\,(0,6,7,8,12,13,14,15)$　　　　　　　10

　　(b)Find the reduced SOP form using K-map　　　　　　　5

　　　$F(A,B,C,D) = \Sigma M\,(0,6,7,8,12,13,14,15)$
　　　Implement using only NAND gates
　　(c) Explain the term " noise margin" and its values for TTL and CMOS families.　5

4. (a) Design and explain 8 bit binary adder using IC 7483 — 10

(b) Design an clocked MN flip-flop using JK flip-flop. The function table of — 10
MN flip-flop is as follows:

M	N	Q_{n+1}
0	0	Q_n'
0	1	0
1	0	1
1	1	Q_n

5. (a) Explain and draw MOD – 10 asynchronous counter using T- FF. — 10
Draw output waveforms and show where glitches occur.

(b) A parking lot has 4 parking slots. A car requires 1 empty slot, a tempo — 10
requires 2 empty adjacent parking slots and a truck requires 3 empty adjacent
parking slots. Each slot has a sensor which indicates a '1' when slot is full and
indicates a '0' when slot is empty. Generate 3 outputs: car, tempo and truck
which indicate which vehicle should be allowed to park.

6. (a) Construct a ring counter using IC 74194 and draw the output waveforms. — 10

(b) Consider the expression $Y = AD' + BD$. Find out whether any hazard exits — 10
in the hardware implementation. If yes, eliminate the hazard.

7. (b) Draw and explain a 9 - bit even parity checker using IC 74180 — 10

(a) Implement the function using single IC 74151 and some gates — 10
$F = \Sigma m (1,2,4,7,10,13,14)$