3/6/2011

BE ETRX VII (Rev)
VLSI Design

Con. 3447-11. **(REVISED COURSE)** **RK-3336**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary**.

1. (a) Draw the stick diagram and mask layout using λ based design rules for a depletion load nMOS inverter with pull up to pull down ratio as 4:1 (i.e. $\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$). (10)

   (b) Assuming that the work function of the metal is smaller than that of a p-type semiconductor, pictorially depict the cross sectional view and energy band diagram for an n-channel MOS transistor under the following conditions: (10)

   (i) When the metal and semiconductor are shorted
   (ii) Flat band condition
   (iii) When the surface is depleted of carriers
   (iv) Onset of inversion at the surface
   (v) When the semiconductor surface is accumulated with majority carriers.

2. (a) Explain the complete fabrication process steps for a CMOS inverter using p-well process with the help of cross sectional diagrams for all important masking steps. (10)

   (b) Calculate the threshold voltage V_{T0} at V_{SB} = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: (10)

   Substrate doping, $N_A = 10^{16}/\text{cm}^3$
   Polysilicon gate doping, $N_D = 2 \times 10^{20}/\text{cm}^3$
   Gate oxide thickness, $T_{OX} = 500\ A^0$.
   Oxide interface fixed charge density, $N_{OX} = 4 \times 10^{10}/\text{cm}^2$

   Also calculate the ion implant dose necessary to change the threshold voltage from V_{T0} to V_T = -1 V and comment on the result.

3. (a) Implement the following Boolean function in CMOS logic: (10)
   $Y = \overline{A(D+E)+BC}$
   Draw the stick diagram for the circuit.

   (b) Derive an expression for the inverter threshold voltage (switching voltage) of a CMOS inverter. Calculate the (w/L) ratios of the nMOS and pMOS transistor in the CMOS inverter circuit with the following parameters: (10)

   NMOS $V_{Tn} = 0.6$ V, $\mu_{ncox} = 60\ \mu A/V^2$,
   PMOS $V_{Tp} = -0.8$ V, $\mu_{pcox} = 20\ \mu A/V^2$,
   $V_{DD} = 3$ V, $V_{TH} = 1.5$ V

4. (a) Compare Resistive load, Depletion load and Enhancement load inverters. Also write their merits, demerits and applications. (10)

   (b) Design a half adder circuit using primitive gates. Using the half adder blocks designed & required primitive gates, design a full adder circuit. Write verilog codes for both the circuits designed and a Test bench to test the functionality of the full adder. (10)

5. (a) Explain various sources of power dissipation in digital CMOS circuits with the help of appropriate diagrams and expressions. (10)

   (b) Consider an n-channel MOSFET with W = 15 μm, L = 2 μm and $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2. Assume that the drain current in the non saturation region for $V_{Ds} = 0.10$ is $I_D = 35$ μA at $V_{Gs} = 1.5$ V and $I_D = 35$ μA at $V_{Gs} = 2.5$ V. Determine the inversion carrier mobility and the threshold voltage of the n-MOSFET. (10)

6. (a) Explain constant voltage and constant field scaling in detail with their merits and demerits. (10)

   (b) Design a clocked SR latch using CMOS technology and write verilog code for the circuit. (10)

7. Write short notes on any three: (20)

   (a) CMOS latch up & its prevention
   (b) Buried and Butting contacts
   (c) Ion implantation
   (d) MOS capacitance .