M.E. Sem I (Rev.) Etrx. Digital Sys. Design 18/12/08

Con. 5216-08. BB-8216

(REVISED COURSE)

(4 Hours) [Total Marks : 100

N.B.: (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume **suitable** additional data if **required.**
(4) **Figure** to the **right** indicte **full** marks.

1. (a) Design a circuit which makes optimum utilization of a selected PLA to implement the following functions. 8

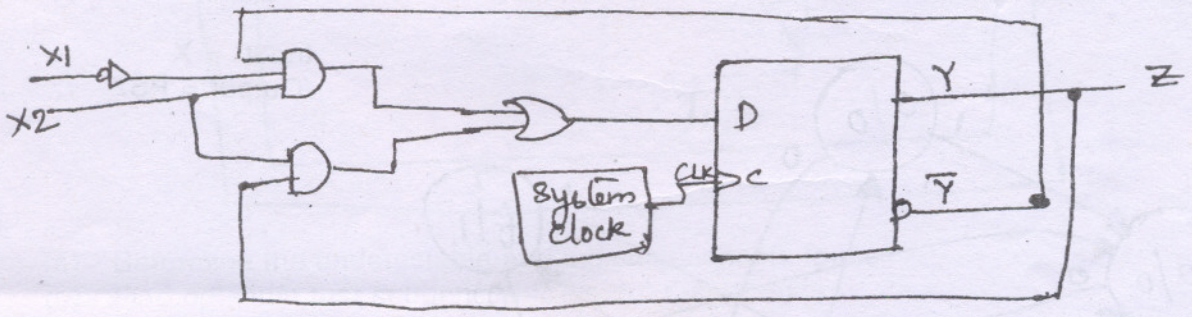
$F_1 = \sum m\ (0, 1, 2, 3, 6, 9, 11)$

$F_2 = \sum m\ (0, 1, 6, 8, 9)$

$F_3 = \sum m\ (2, 3, 8, 9, 11)$

Specify the correct size of PLA used for optimum utilization.

(b) Analyze the state machine shown in **figure** below and obtain the following :— 12
(i) The excitation input and external output equations
(ii) The flow may
(iii) The state diagram.



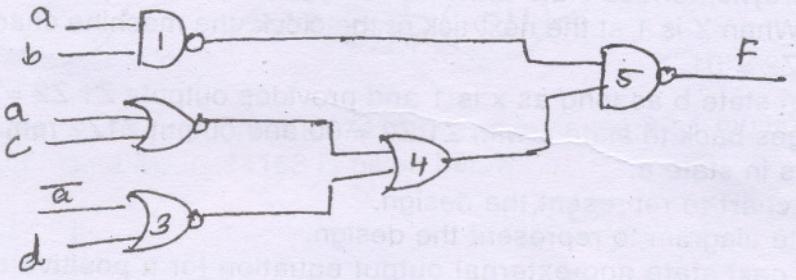
2. (a) Implement the following sets of functions using a decoder. Utilize OR elements with the smallest possible number of inputs (fanin) that is count IS and OS and use the smallest number. Use the divide and conquer approach. 10

$F_1(A, B, C) = \sum m\ (0, 1, 2)$

$F_2(A, B, C) = \sum m\ (1, 2, 3, 4, 5, 7)$

$F_3(A, B, C) = \sum m\ (2, 3, 5, 7)$

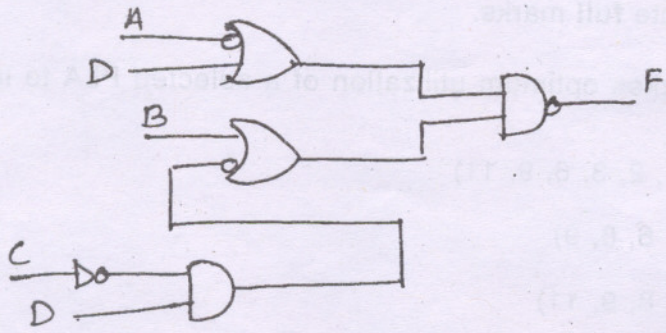
(b) Find all the static hazard in the following circuit. For each hazard, specify the values of input variable and which variable is changing when hazard occurs for one of the hazard specify the order in which the gate output must change. 10



[TURN OVER

3. (a) Design a Parity Generator/Parity checks circuit such that the same circuit can perform the task of either parity generation or parity checking. A system will utilize your design to transmit seven information bits plus a parity bit. Design your circuit so that it can also be used in either an odd or even parity system. **10**

(b) Using the path sensitization technique determine the input test for the fault p-a-1 in the circuit and check the answer using Boolean difference method. **10**

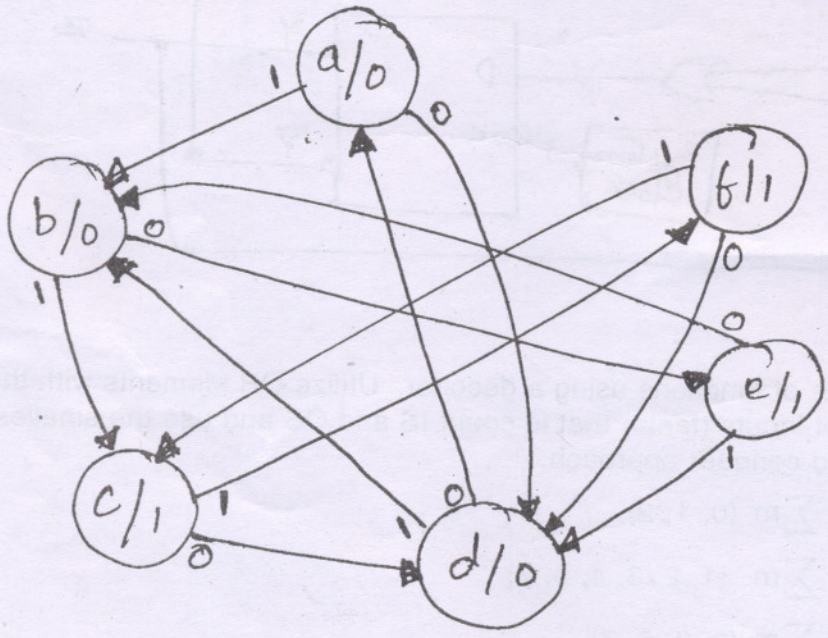


4. (a) Consider the Moore machine shown in **figure** **12**

(i) Obtain its PS/NS table

(ii) Check for redundant states. What is the minimum number of flip-flops required for this machine before and after reduction.

(iii) Implement the circuit diagram using D flip-flop.



(b) Design a circuit to implement a XS-3 to BCD code converter using PROM. The signal list for the code converter is I_3, I_2, I_1, I_0, F_3, F_2, F_1, F_0. **8**

5. Design a Mealy type synchronous state machine with one external input x and Two external outputs Z1 and Z2. When X is 1 at the next tick of the clock, the machine changes from state a to state b and Z1 Z2 = 01. **20**

The machine stays in state b as long as x is 1 and provides outputs Z1 Z2 = 10. When x is 0 the machine changes back to state a with Z1 Z2 = 00 and output Z1Z2 remains 00 as long as the machine stays in state a.

(a) Draw ASM chart to represent the design.

(b) Draw a state diagram to represent the design.

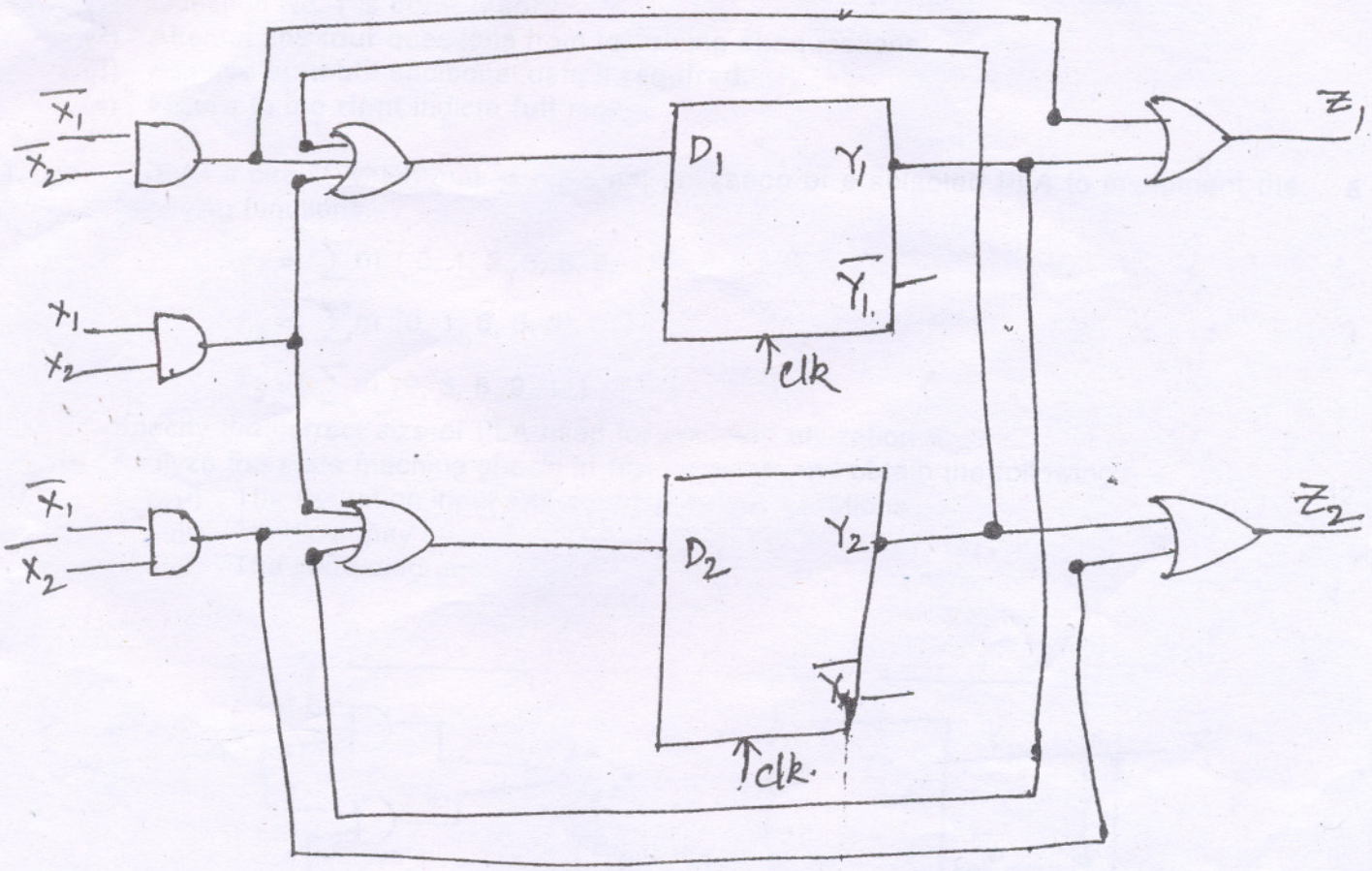
(c) Obtain the next state and external output equation for a positive edge-triggered D flip-flops using either (a) or (b).

(d) Minimize the equation and draw the circuit diagram.

6. Consider the following faults of the circuit shown in **figure** below : 20

(i) All possible single s-a-0 faults occurs at the input of each of the AND gates.

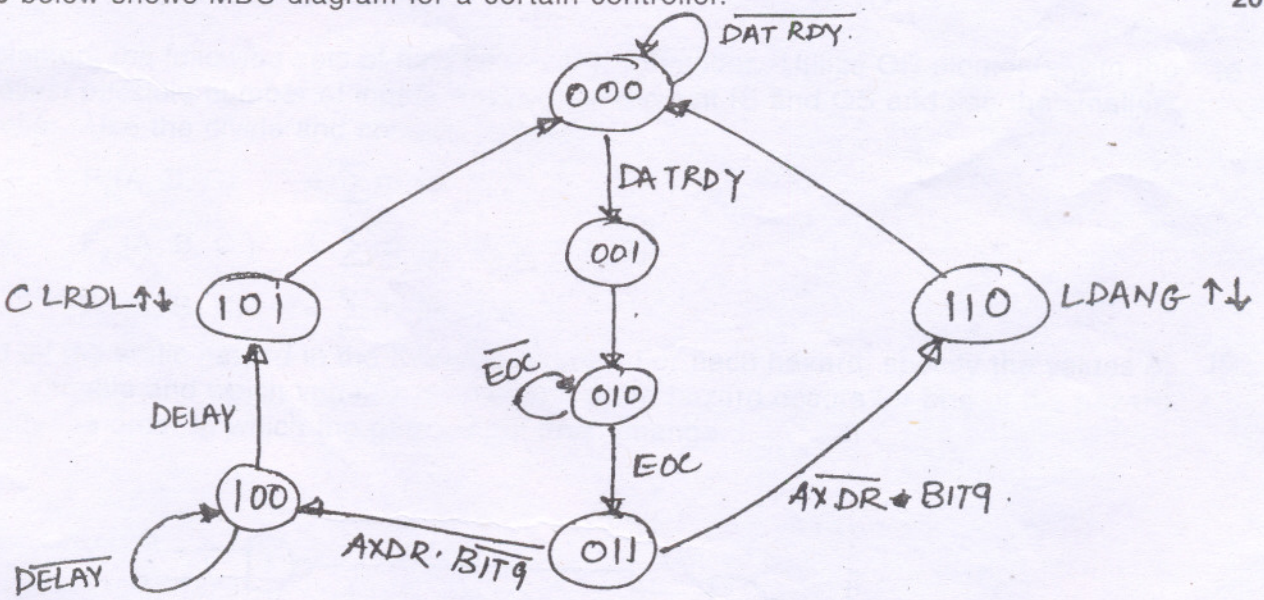
(ii) All possible single s-a-1 faults occurs at the output of each of the OR gates.



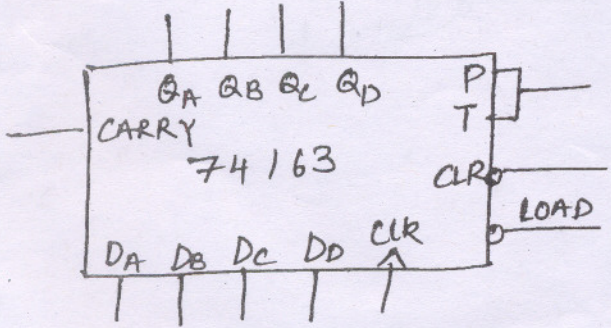
(a) Determine the undetectable and indistinguishable faults

(b) Find optimum test sequences to detect these faults.

7. **Figure** below shows MDS diagram for a certain controller. 20



Design the controller using counter IC 74163. You may use 8 : 1 multiplexers and additional gates if required. Data for IC 74163 is given below :



CLK	LOAD	PT	
0	X	X	Clear
1	0	X	Load
1	1	0	No change
1	1	1	Increment count