BE | ETRX | VII (R) 21/5/13
VLSI Design

D:sneha (B) April 2013 102

Con. 8903–13. GS–5530

## (REVISED COURSE)

(3 Hours) [ Total Marks : 100

**N.B.** (1) Question No. **1** is **compulsory**.
(2) Attempt any questions **four** out of remaining **six** questions.
(3) Assume suitable **data** wherever **necessary** and state it **clearly**.

1. Attempt any **four** :– **20**
   (a) Discuss why the threshold voltage changes when a reverse-biased source-to-substrate voltage is applied to a MOSFET.
   (b) Consider on MOS structure with a p-type semiconductor substrate doped to $N_a = 10^{16}/cm^3$, a silicon dioxide insulator with a thickness of 500 A°, an $n^+$ polysilicon gate doped to $2 \times 10^{20}/cm^3$ and oxide-interface charge density of $4 \times 10^{10}/cm^2$ calculate the flat band voltage.
   (c) Explain the λ(lambda) based design rule for an implant mask in nMOS technology and the problems faced in case of violation of the rule during fabrication. Draw appropriate diagrams.
   (d) Discuss various steps of Silicon Planar Process and its advantage in fabrication of Integrated circuits.
   (e) Design a 4:1 MUX using nMOS pass transistor logic and discuss the drawbacks of the circuit and the remedies to overcome the drawbacks.

2. (a) Sketch and explain the general shape of the low frequency C-V characteristics to be expected from a metal-oxide-p-substrate capacitor. How does the characteristic change for the high frequency condition ? **10**
   (b) Consider an n-channel MOSFET with gate width $w = 10\mu m$, gate length $L = 2\mu m$, and oxide capacitance $C_{ox} = 10^{-7}$ F/cm². In the linear region, the drain current is found to have the following values at $V_{DS} = 0.1V$ : **10**
   $I_D = 50\ \mu A$ at $V_{GS} = 1.5$ V
   $I_D = 80\ \mu A$ at $V_{GS} = 2.5$ V
   Calculate the inversion carrier mobility and the threshold voltage of the device.

3. (a) What do you mean by inverter ratio ? Derive the same for a CMOS inverter and discuss symmetric CMOS inverter design. **10**
   (b) A PMOS transistor is to be fabricated. Describe its fabrication steps giving the mask sequence. Sketch the cross sectional view of all the masking steps. **10**

4. (a) Draw the stick diagram and mask layout using λ based design rules for a depletion load nMOS inverter with pull-up to pull-down ratio as 4:1 $\left(\text{i.e.} \frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}\right)$ **10**

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(b) Determine the device sizes for 3-input NAND and 3-input NOR gates in conve[illegible] CMOS. Assume that the basic inverter is sized as $\left(\frac{W}{L}\right)_n = 1, \left(\frac{W}{L}\right)_p = 2$ and t[illegible] goal of the design is to have NAND 3 and NOR 3 gates with the same [illegible] characteristics as the inverter. What problems arise if the number of fanins ([illegible] is increased to 10 ?

5. (a) Compare the full scaling model with constant voltage scaling model for MOSFETS. 10
Demonstrate clearly the effects of scaling on the device density, speed of the c[illegible] power consumption and current density of the gates.

(b) A depletion load nMOS inverter has following parameters : 10

$\mu nC_{ox} = 30\ \mu A/V^2$, $V_{TO} = 0{\cdot}8V$ (enhancement type)

$V_{TO} = -2.8V$ (depletion type), $r = 0.38\sqrt{V}$

$|2\phi_f| = 0.6V$, $V_{DD} = 5V$

(i) Determine the $\left(\frac{W}{L}\right)$ ratios of both transistors such that the static (D[illegible] power dissipation for $V_{in} = V_{OH}$ is 250 mW, and $V_{OL} = 0.3V$.

(ii) Calculate $V_{IL}$ and $V_{IH}$ values and determine the noise margines.

6. (a) Implement the circuit for clocked SR-latch at switch level and write verilog module for the circuit designed.

(b) Implement the following function using CMOS technology $F=\overline{XYZ+XW}$. Also draw the stick diagram for the circuit designed.

7. Write short notes (attempt any **two**) :–
   (a) 4 × 4 barrel shifter
   (b) Short channel effects
   (c) CMOS latch-up and its prevention.

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