Code No. : 5346/S

# FACULTY OF INFORMATICS

## B.E. 2/4 (IT) I Semester (Suppl.) Examination, July 2012

## DIGITAL ELECTRONICS AND LOGIC DESIGN

Time : 3 Hours] [Max. Marks : 75

***Note :*** *1) Answer **all** questions from Part – **A**.*
*2) Anwer **any five** questions from Part – **B**.*

PART – A **(25 Marks)**

1. Write the advantages of designing custom chips. **2**
2. Implement XOR gate using NOR gates only. **3**
3. Illustrate practical applications of multiplexers. **3**
4. Mention the differences between PAL and PLA. **2**
5. Explain the operation of Basic Latch using Truth Table. **3**
6. Mention the difference between D flip-flop and F flip-flop. **2**
7. What are the elements of ASM chart ? **2**
8. Write the basic design steps involved in design of synchronous sequential circuits. **3**
9. Explain setup time and hold time of flip flop. **3**
10. What is a Hazard ? Explain their types. **2**

PART – B (50 Marks)

11. Reduce the following expression to minimum lost SOP, draw the logic circuit using NAND gates only and write the corresponding VHDL code.

$f(x_1, x_2, x_3, x_4) = \sum m(5, 6, 9, 10, 12, 13, 14, 15) + d(2, 4)$ 10

12. a) Explain the architecture of Complex Programmable Logic Device (CPLD). 6

b) Draw the 4 : 1 MUX diagram and write VHDL code for 4 : 1 multiplexer. 4

13. a) Explain the operation of Parallel Access Shift Register. 5

b) With a neat diagram explain the negative type master slave edge triggered D flip-flop. 5

14. Explain FSM as an Arbiter circuit. 10

15. Explain the ASM chart and data path circuit for "Shift and Add multiplier ". 10

16. a) Explain the design process and design of Digital Hardware Unit. 6

b) Write short notes on CAD tools. 4

17. a) Formal model of a synchronous sequential circuit. 4

b) Combinational Circuits Vs Sequential Circuits. 3

c) State Moore's law and its significance. 3