UNIT - II

Transistor and its Applications

Transistor and applications : working Principle of BJT, FET and MOSFET & CMOS application of BJT and MOSFET as amplifier and Switch.

Transistor :- ⇒ Transferred + Resistor.

* PN Junctions are examples of 2 terminal 1 Junction devices. There is a one interface between the two components.

* A transistor is a example of 3 terminal 2 Junction device.

* The name transistor is derived from transfer resistance.

* In Active mode. Junction 1 acts in F.B Junction 2 acts in R.B (Reverse Bias)

* Transferred Resistance from low to high so it acts as amplifier, and Switch.

BJT :- Bipolar Junction Transistor :-

BJT is a three terminal doped Semiconductor Device, and it amplify the week Signals, also used in Switching operation. So BJT used in both digital and analog applications.

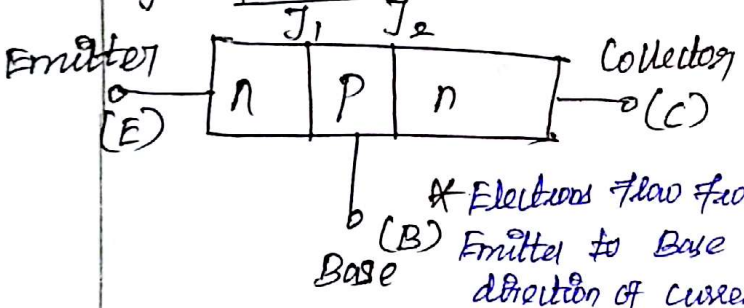
Physical Structure of BJT :-

⇒ Two types of BJT.

* npn Transistor ⇒ P-type Semiconductor material is Sandwiched b/w two n-type Semiconductor material
* pnp Transistor. ⇒ N-type material is Sandwiched b/w two P-type material

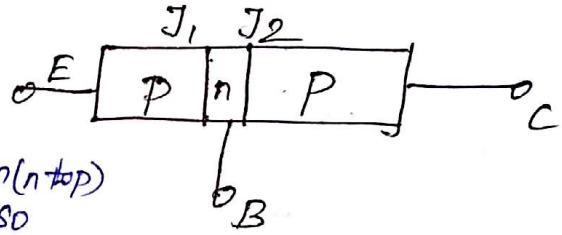
⇒ i) Two pn diodes are connected back to back by np & pn in npn (or) pn & np in pnp transistor.

Fig:- npn transistor



* Electrons flow from (n top) Emitter to Base so direction of current is B to E

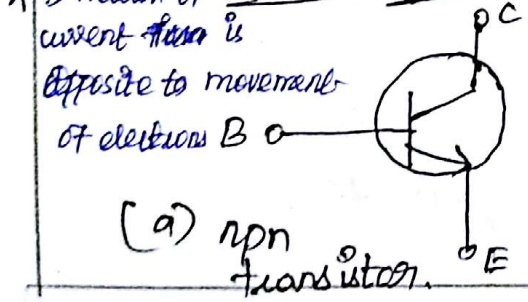
Fig: Pnp transistor



1) three regions ⇒ Emitter region, base region, collector region.
2) Two Junctions ⇒ Emitter Base Junction collector Base Junction.
3) Three Terminals ⇒ Emitter, Base, collector.

Transistor Symbols:

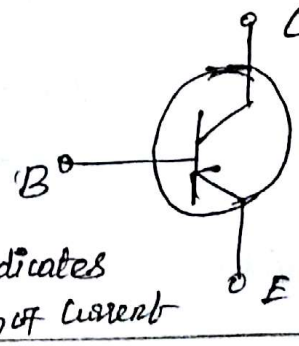
* Direction of current flow is opposite to movement of electrons



(a) npn transistor.

Arrow indicates direction of current flow

* electrons flow from B to E so current flow from E to B



(b) pnp transistor

Emitter region	Base region	Collector region
Heavily doped	lightly doped	Moderatly doped
Medium width	width is low	High width

* Collector region width is very high because it has to collect electrons and heat is produced in it so width is more, better heat dissipation will be there

width :- C > E > B, doping :- E > C > B

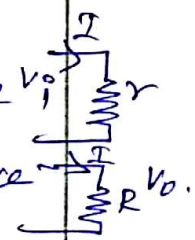
Bipolar ⇒ Two types of charge carriers they are electrons & holes, so two types of Polarities

Junction ⇒ It is connecting point of two type materials

Transistor ⇒ Transfer + Resistor.

* Junction J_1 ⇒ Forward biased ⇒ low resistance

J_2 ⇒ Reverse biased ⇒ high resistance



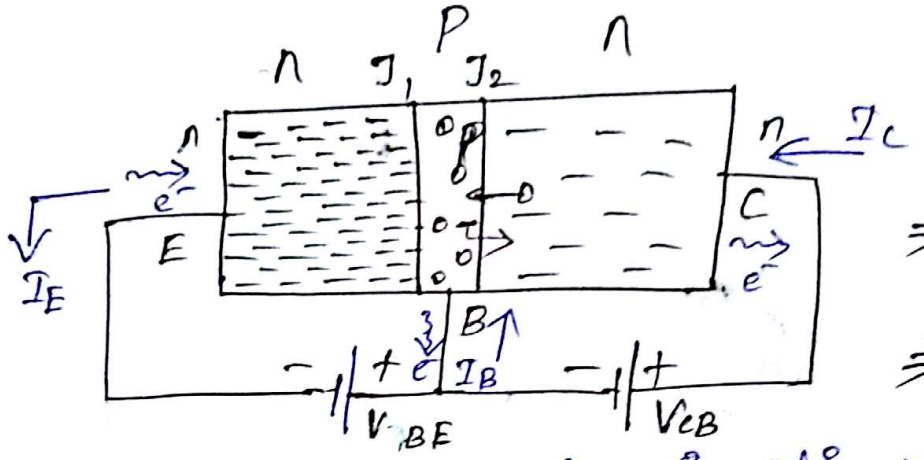
$V_i = Ir$

$V_o = IR$

* weak signal introduced to low resistance output is taken from high resistance. [$V_i < V_o$ amplification of S/L]

Junction J_1 (EB)	Junction J_2 (CB)	Operating Region	Transistor Operates as
F·B	R·B	Active region ⇒	Amplifier
F·B	F·B	Saturation mode	Logical "ON" (or) closed
R·B	R·B	Cut off region	"OFF" (or) open circuit
R·B	F·B	Inverted	Switching emitter & collector Rarely used

Operation of BJT:-



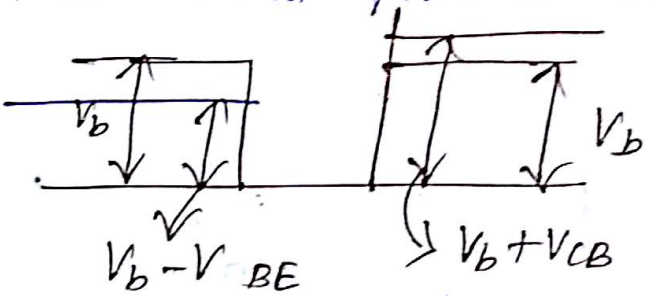
⇒ F·B Potential V_{BE}

⇒ R·B potential V_{CB}

* To operate transistor in active mode, J_1 ⇒ F·B, need to apply +ve voltage to +ve terminal (Base). J_2 ⇒ R·B so +ve voltage to -ve terminal (collector)

* V_b ⇒ Barrier Potential for Junction J_1 & J_2 when transistor is open circuited (or) no biasing voltage

* If we apply biasing voltage to transistor, the barrier Potential becomes,



In F·B it is decreased

In Reverse bias V_b is increased to $V_b + V_{CB}$

* Barrier potential at Junction J_1 is reduced So electrons cross over J_1 to base, Very small amount of electron only recombined with base, because base is Very Small and lightly doped

* So most of electrons will cross J_2 to the collector.

$\Rightarrow$ N no of electrons enter into base from Emitter

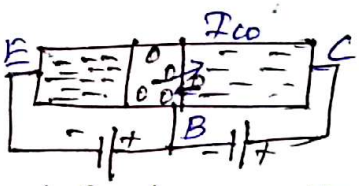
$\Rightarrow (1-\alpha)N$ no of " combined with base

$\Rightarrow \alpha N$ no of " move to collector.

* So only 2 to 5% electrons combined in base

* 98 to 95% electrons move to collector

* Most of electrons emitted by emitter is move to collector, this is operation when Junction is forward biased in transistor.



Reverse Saturation current:-

Junction J_2 is reverse biased so there is reverse saturation current. (or) leakage current I_{CO}

$I_{CO} \Rightarrow$ open circuit

$\Downarrow$

current with collector.

$I_C = \alpha I_E + I_{CO}$ (α times Emitter current (αN electrons moving to collector))

$$\boxed{I_C = \alpha I_E + I_{CO}}$$

From KCL:

Sum of currents entering = Sum of Currents leaving

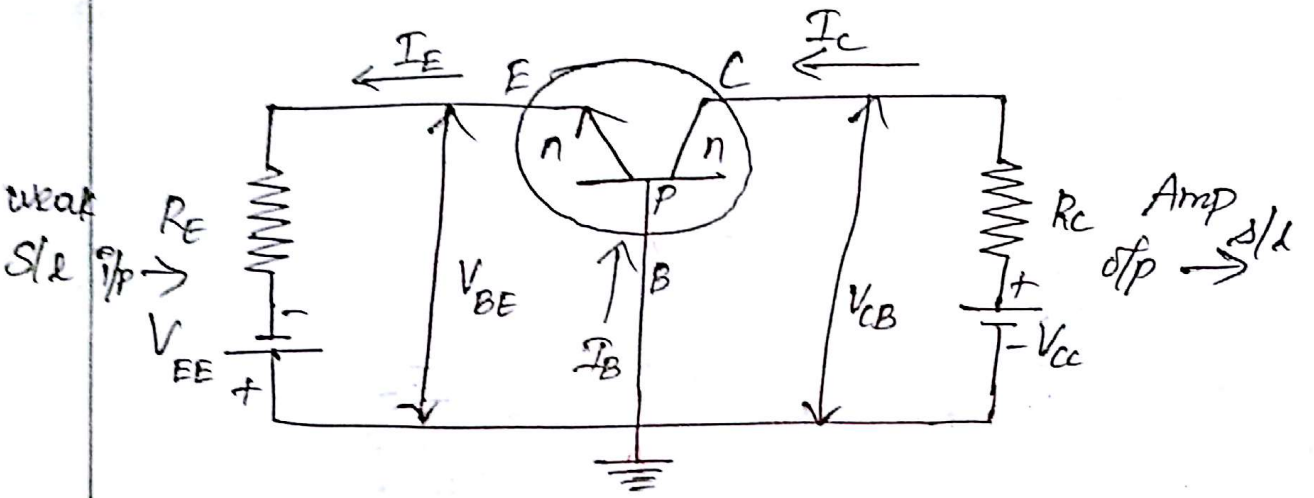
$I_B + I_C = I_E$

$$\boxed{I_E = I_B + I_C}$$

Based on three terminals three types of Configurations :-

1) Common base Configuration
2) common Emitter "
3) common collector "

Common Base Configuration of Transistor :-



* In common base configuration base is common to input and output circuit, by Symbol of Emitter, this transistor is npn transistor. Base is grounded.

* Emitter is input side because weak S/l is introduced in 'E' Side and amplified S/l on 'C' side is only on transistor in active mode

i) $J_1 \Rightarrow F\cdot B \Rightarrow \overset{n}{E}\overset{P}{B}$ diode $\Rightarrow$ so B to +ve terminal, E to -ve "

ii) $J_2 \Rightarrow R\cdot B \Rightarrow \underset{P}{B}\underset{n}{C}$ diode $\Rightarrow$ B to -ve terminal, C to +ve "

In Diode $\Rightarrow$ Simple VI characteristics

In transistor $\Rightarrow$ I/p & o/p characteristics

$V_{BE} \neq V_{EB}$ high Potent

because B has +Ve V

E has -Ve V low Potent

$V_{CB} \neq V_{BE}$

Input Charac I_E V/s V_{BE}

i/p current — o/p voltage

Output Charac I_C V/s V_{CB} ⇒ o/p voltage

o/p current

$V_{BE} = V_{EE}$ (If R_E neglect)

$V_{CB} = V_{CC}$ (If R_C neglect)

From KCL :- $\boxed{I_E = I_C + I_B}$ (For Active mode)

$\boxed{I_C = \alpha I_E + I_{CBO}}$ — common Base configuration

I_{CBO} → open circuit current in collector region

$I_E \gg I_{CBO}$ because Reverse Saturation current due to minority charge carriers, Very small in number. (neglect I_{CBO})

$I_C = \alpha I_E$

Gain = $\frac{o/p}{i/p}$

$\alpha = \frac{I_C}{I_E} \frac{o/p}{i/p}$

$\boxed{\alpha = \frac{I_C}{I_E}}$

'α' — common base Current gain. (or) Amplification factor

'α' b/w ⇒ 0.95 – 0.98.

i.e) 95% to 98% Emitter current is Collector current

So 5% to 2% recombination current in Base

$\boxed{I_B = (1-\alpha) I_E}$

Input characteristics :- [F·B Diode]

Graphical relation between i/p current and o/p voltage for different o/p voltages.

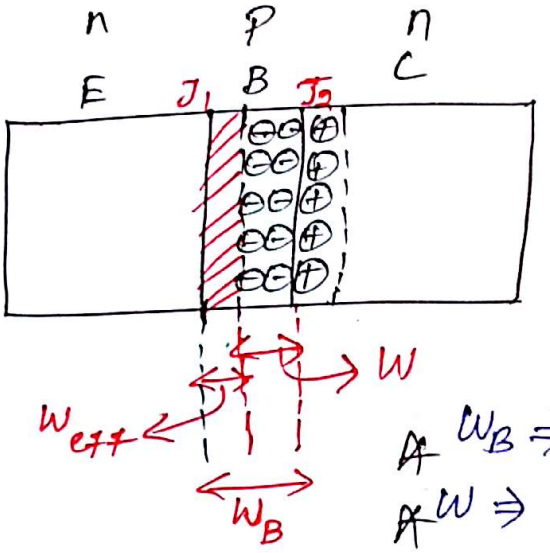
i.e. I_E Vs V_{BE} for diff V_{CB}

Input characteristics is similar to Forward biased diode

Effect on characteristics is defined interms of Early effect :-

also named as base width modulation.

* when increase in voltage V_{CB} there is a modulation in base width



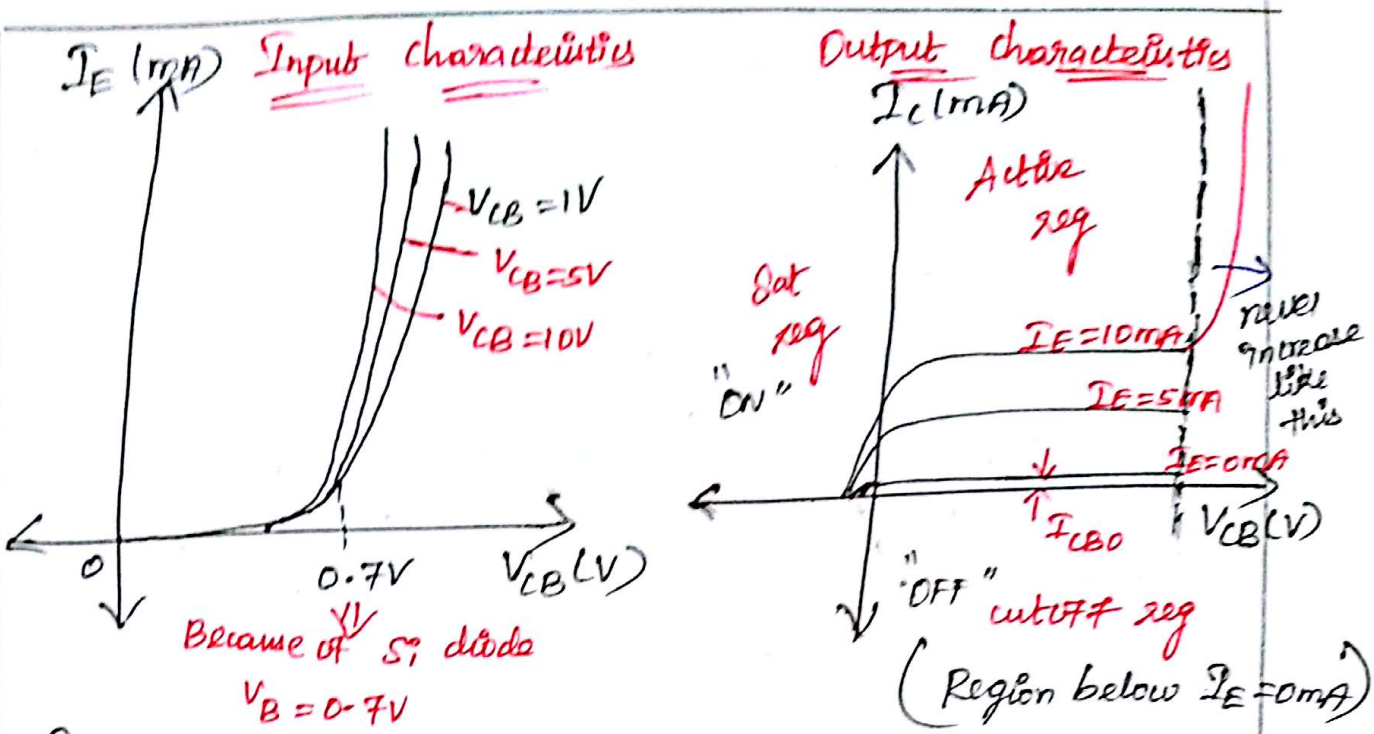
* $J_1 \Rightarrow$ F·B
* $J_2 \Rightarrow$ R·B $\Rightarrow$ width of depletion layer increases
* In reverse bias depletion layer is more in base region because of lightly doped
* $W_B \Rightarrow$ width of base region
* $W \Rightarrow$ " " depletion layer Penetrated in base region
* $W_{eff} \Rightarrow$ width of region with no depletion layer in base

$W_B = W_{eff} + W$

$$W_{eff} = W_B - W.$$

* $V_{CB} \uparrow \Rightarrow W \uparrow_{es} \Rightarrow W_{eff} \downarrow_{es}$ chance of recombination Place W_{eff} is $\downarrow_{es}$ so $I_E \uparrow_{es}$

$\Rightarrow$ So By increasing V_{CB} o/p voltage the Input current I_E also increases



Output characteristics:-

* Graphical representation between o/p current and o/p voltage for different i/p current

Eg) I_C V_S V_{CB} for Various Current I_E

* Output characteristics is similar to reverse biased diode

W.K.T, $I_C = \alpha I_E + I_{CBO}$ (independent of V_{CB})

$I_C = \alpha I_E$ $(\because I_E >> I_{CBO})$

$I_C \approx I_E$ $(\because \alpha = 0.95 - 0.98 \approx 1)$

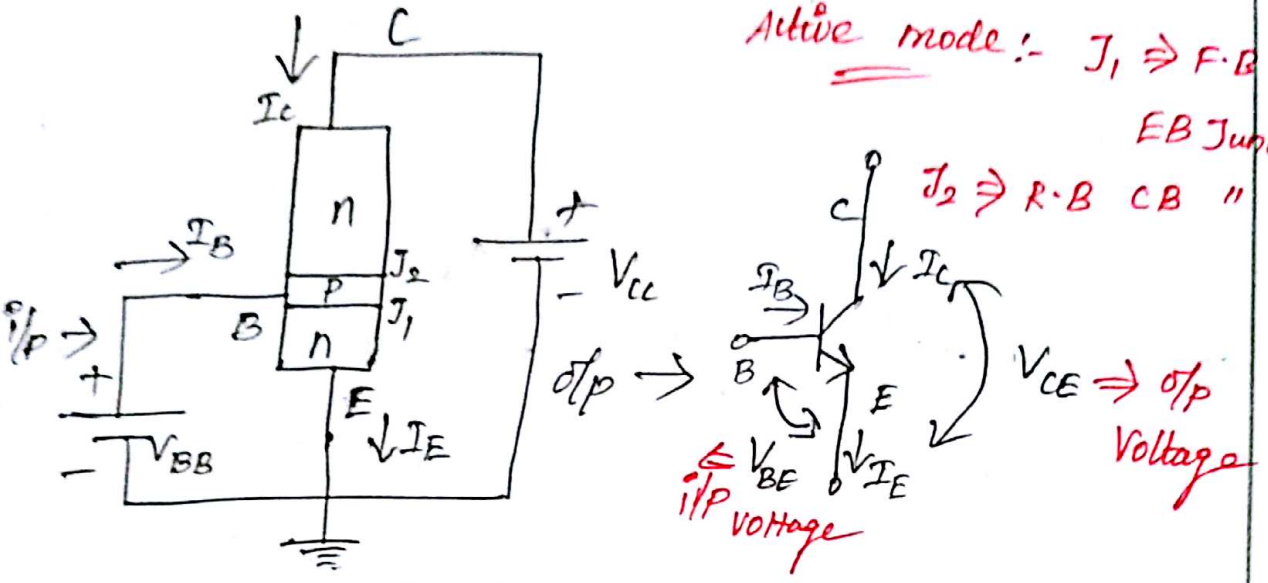
* So o/p current affects by input current

* If I_E = 0mA then $I_C = I_{CBO}$

* If increase in V_{CB} Breakdown will occur in reverse bias condition [$V_{CB} \uparrow$ es ⇒ rapidly $I_B \uparrow$ es

* This situation never likes because transistor can't withstand in high power dissipated

Common Emitter configuration of transistor :-



In Common Emitter configuration, the Emitter terminal is common to input and Output Circuit. Base in i/p side and collector is o/p side.

w.k.t, $I_E = I_C + I_B$ — ①

$I_C = \alpha I_E + I_{CBO}$ — ②

Sub eqn ② in ①

$I_C = \alpha [I_C + I_B] + I_{CBO}$

$I_C = \alpha I_C + \alpha I_B + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$(1-\alpha) I_C = \alpha I_B + I_{CBO}$

$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$\left[\because \frac{\alpha}{1-\alpha} = \beta \quad \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{\alpha + 1 - \alpha}{1-\alpha} = \frac{1}{1-\alpha} \right]$

$$I_c = \beta I_B + (\beta + 1) I_{CBO}$$

Case 1 :- $\alpha = 0.98$ Case 2 :- $\alpha = 0.95$

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$ $\beta = \frac{0.95}{1-0.95} = 19$

* Slit change in "α" vary large change in "β"

* $\alpha \Rightarrow$ is amplification factor in common base configuration

$\alpha < 1$

* $50 \leq \beta \leq 400$

$I_C = \beta I_B + (\beta+1) I_{CBO}$

$I_C = \beta I_B + I_{CEO}$ $\Rightarrow$ Reverse Sat current in common Emitter config

$I_C = \beta I_B$

$\beta I_B \gg I_{CEO}$

$\beta = 100$

Ex: $I_B = 1mA$ $\beta = \frac{I_C}{I_B}$

$I_C = \beta I_B = 100mA$

[Amp of o/p current]

$\beta \Rightarrow$ current amplification factor

* Generally transistor works as Voltage amplifier. CE configuration works as Current amplifier

In CB

$I_C = \alpha I_E + I_{CBO}$

In CE

$I_C = \beta I_B + I_{CEO}(1+\beta)$

$= \beta I_B + (\beta+1) I_{CEO}$

Contribution of leakage current is high in CE configuration compared to CB configuration because of $(\beta+1)$ factor.

Input characteristics:-

* Graphical representation between i/p current and i/p voltage for various o/p voltages.

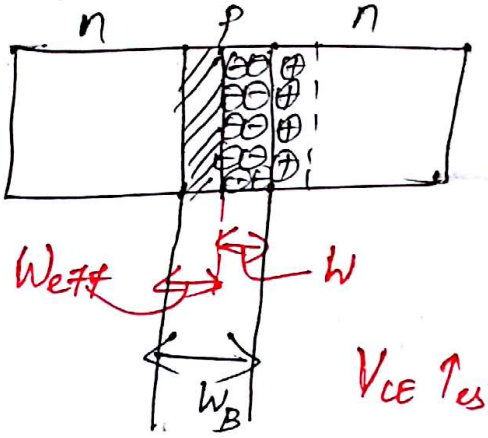
i.e) I_B Vs V_{BE} for various V_{CE}

* Input characteristics is similar to Forward Biased PN diode.

Early Effect:- [Base width modulation]

To find characteristics because of Effects of o/p voltage V_{CE} go to early effect

$V_{BE} > V_b$
Sudden ↑es in current from V_b in FB



$J_1 \Rightarrow$ FB
$J_2 \Rightarrow$ R.B

$W_{eff} = W_B - W$

$V_{CE} = V_{CB} + V_{BE}$

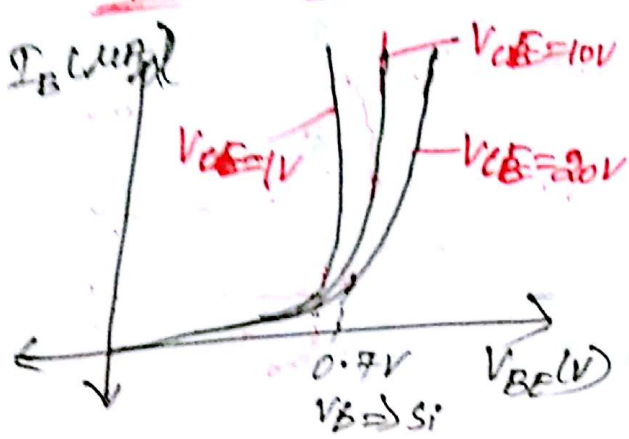
$V_{CE} \uparrow es \Rightarrow V_{CB} \uparrow es \Rightarrow W \uparrow es \Rightarrow W_{eff} \downarrow es$

$W_{eff} \downarrow es \Rightarrow$ Region recombination decreases, So electrons emitted from emitter will not recombine with holes in Base, this will reduce I_B ($\downarrow es$ i/p current)

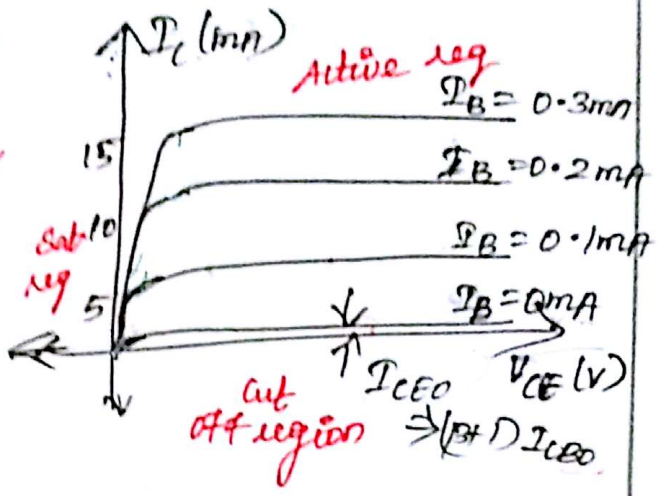
So $V_{CE} \uparrow es$ $I_B \downarrow es$

(or) $V_{CE} \downarrow es$ $I_B \uparrow es$.

Input characteristics



Output characteristics



Output characteristics:-

* Graphical representation between o/p current and o/p voltage for different i/p current

ie) I_C Vs V_{CE} for Various I_B.

w.k.t, $$I_C = \beta I_B + (\beta+1) \cdot I_{CBO}$$

* when, $I_B = 0$, $I_C = (\beta+1)\ I_{CBO}$

$I_C = I_{CEO} \Rightarrow$ leakage current in common emitter configuration

* $I_C \Rightarrow$ independent of o/p voltage V_{CE}; it is depends on I_B

* $I_B = 0.1$ mA , $I_C = 5$mA

$I_B = 0.2$ mA , $I_C = 10$mA

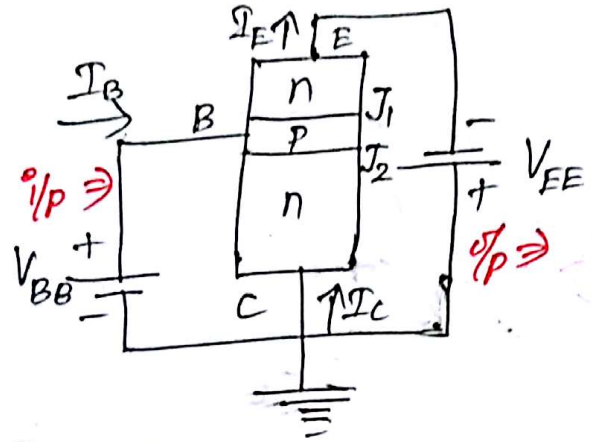
$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{10-5}{0.2-0.1} = \frac{5}{0.1} = 50$$

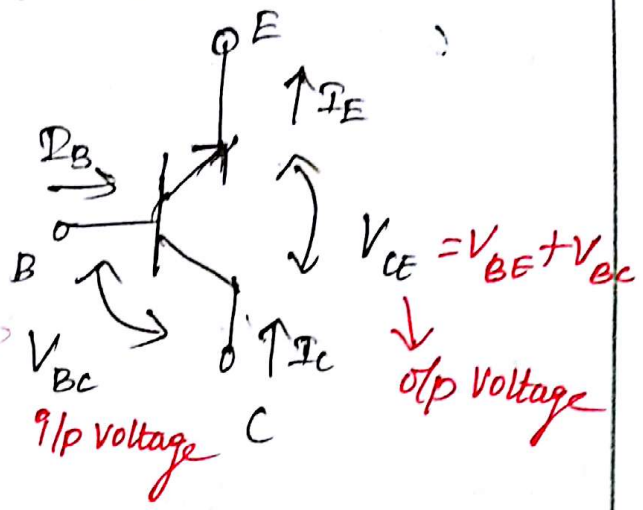
$$\boxed{\beta = 50}$$

* the slope of current is not equal to zero because it depends on V_{CE} also from Early Effect

$V_{CE} \uparrow_{\uparrow} \Rightarrow$ Width $\downarrow_{\downarrow} \Rightarrow I_B \downarrow_{\downarrow} \Rightarrow I_C \uparrow_{\downarrow}$

Common collector configuration of Transistor:-





$J_1 \Rightarrow$ F·B EB Junction

$J_2 \Rightarrow$ R·B CB Junction

In common collector configuration, collector terminal is common to input and Output terminal.

Base is i/p side, Emitter is Output side.

w.k.t, $I_C = \alpha I_E + I_{CBO}$ — ①

$I_E = I_C + I_B$ — ②

Sub eqn ① in eqn ②.

$I_E = \alpha I_E + I_{CBO} + I_B$

$(1-\alpha) I_E = I_B + I_{CBO}$

$I_E = \frac{I_B}{1-\alpha} + \frac{1}{1-\alpha} I_{CBO}$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

"γ" ⇒ current amplification factor in Common collector configuration

$\gamma = \frac{\Delta I_E}{\Delta I_B} \Rightarrow \frac{\text{Change in Emitter current}}{\text{Change in Base current}}$

* In Output Characteristics, the relation between output current I_E and o/p Voltage V_{CE} for different values of i/p current I_B

i) I_E Vs V_{CE} for Various levels of I_B

$I_C = \alpha I_E \quad \alpha = 0.95 - 0.98 \approx 1$

$I_C \approx I_E$

So replace I_E with I_C in o/p Characteristics

* I_C Vs V_{CE} for Various levels of I_B

is nothing but a o/p characteristics of Common Emitter configuration.

So, o/p char of CE = o/p char of CC

* The CC configuration is used for Impedance Matching, because of high i/p Impedance and low o/p Impedance.

Relation Between α, β and γ

Current Gain

1) $\alpha \Rightarrow$ Amplification factor in CB configuration

2) $\beta \Rightarrow$ " " in CE "

3) $\gamma \Rightarrow$ " " in CC "

* Amplification factor is a ratio of output current to the input current.

W.K.T, $\alpha \rightarrow \alpha_{dc} = \frac{I_C}{I_E}$ ——— (1)

$\alpha \rightarrow \alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{const}}$

$\beta \rightarrow \beta_{ac} = \frac{I_C}{I_B}$ ——— (2)

$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{const}}$

$\gamma \rightarrow \gamma_{dc} = \frac{I_E}{I_B}$ ——— (3)

$\gamma_{ac} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE}=\text{const}}$

$I_E = I_C + I_B$

$\div I_B$ $\quad \frac{I_E}{I_B} = \frac{I_C}{I_B} + \frac{I_B}{I_B}$

Sub equn (3) and equ (2) in above eqn,

$\gamma_{dc} = \beta_{dc} + 1$ $\quad$ (or) $\quad \frac{I_E}{I_C} = \frac{I_C}{I_B} + \frac{I_B}{I_C}$

$\boxed{\gamma = \beta + 1}$ $\quad \frac{1}{\alpha} = 1 + \frac{1}{\beta}$

$\boxed{\beta = \frac{\alpha}{1-\alpha}}$

W.K.T $\beta = \frac{\alpha}{1-\alpha}$ Sub in above eqn,

$\gamma = \frac{\alpha}{1-\alpha} + 1$

$= \frac{\alpha + 1 - \alpha}{1-\alpha}$

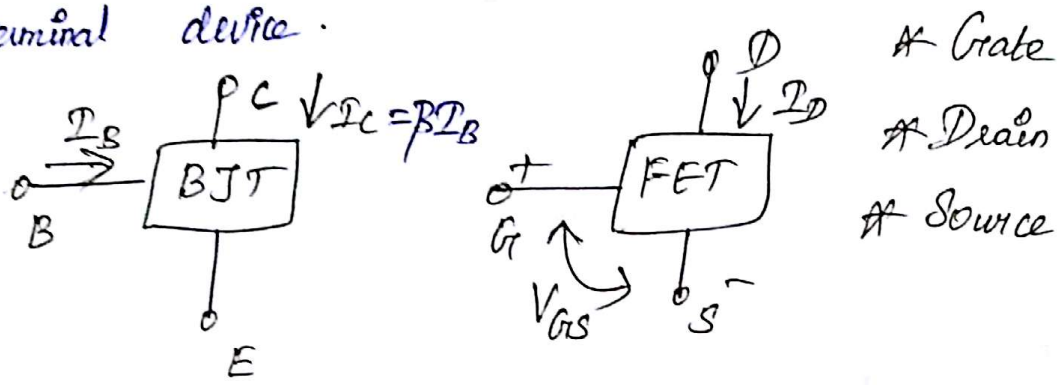
$\boxed{\gamma = \frac{1}{1-\alpha}}$

$\boxed{\gamma = \beta + 1 = \frac{1}{1-\alpha}}$

(Q.) This is Current amplification factor relationship in CE, CB, CC, configuration.

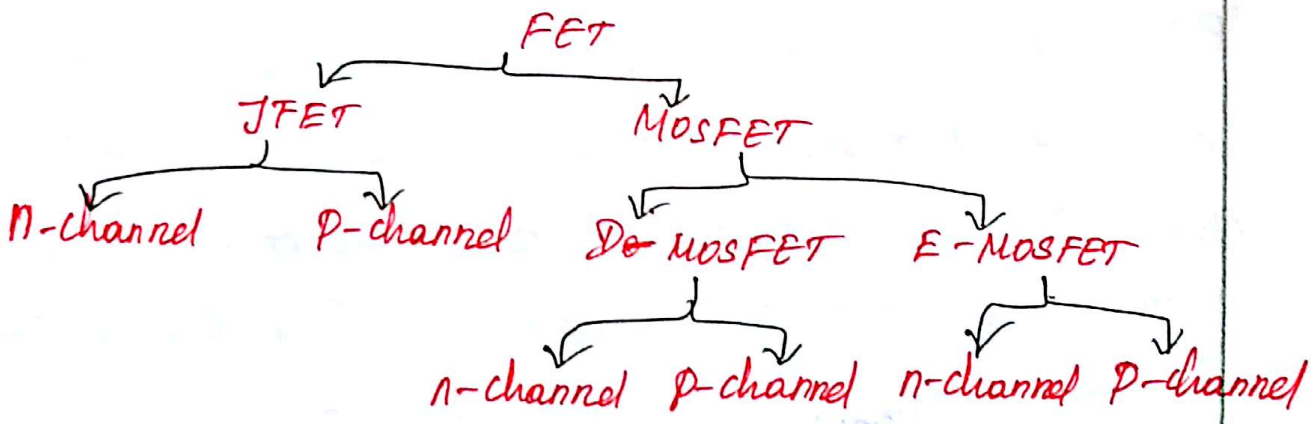
Field-Effect Transistor:- (FET)

* Like a BJT, FET is also a three terminal device.



* Gate
* Drain
* Source

BJT	FET
* BJT is a Current controlled device (∵ o/p current depends on i/p current) $I_C = f(I_B)$	* FET is a Voltage Controlled device (I_D depends on V_{GS}) $I_D = f(V_{GS})$
* BJT is a Bipolar Device (npn transistor & pnp transistor)	* FET is Unipolar Device (n-channel & P-channel)
* Application :- Amplifier & Switch	* Appln :- Amplifier & switch.



"Field effect" ⇒ Electric field is develop by the charges present and it controls the conduction path of the o/p circuit. So there is "effect" due to this field."

JFET :- Junction field effect transistor :

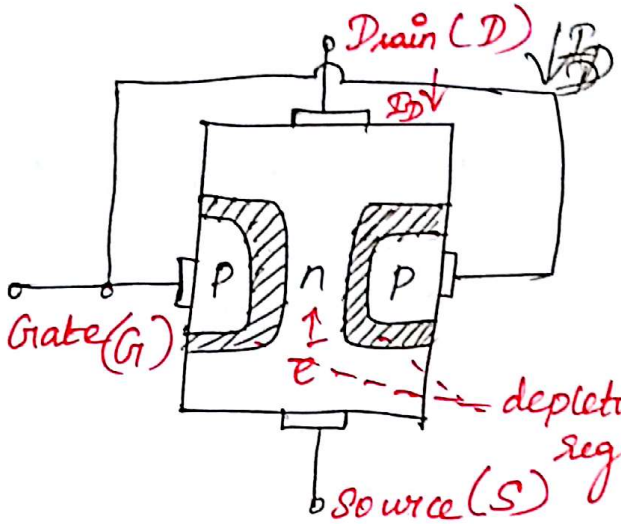


fig:- n-channel FET

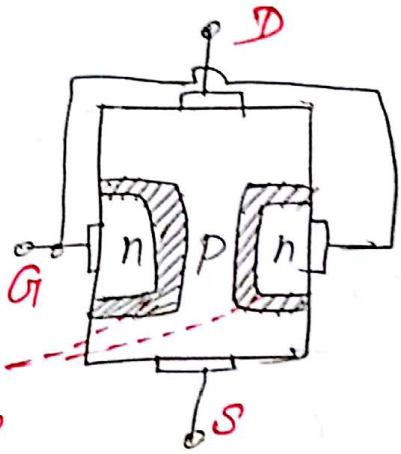


fig :- P-channel FET

* n-type material, forming a channel between two p-type material ⇒ n-channel

* JFET is also a three terminal semiconductor device.

* If depletion layer width increases, then width of n-channel will reduce, because of this there will be obstruction in the flow of electrons. when connect drain and source terminals to a potential difference.

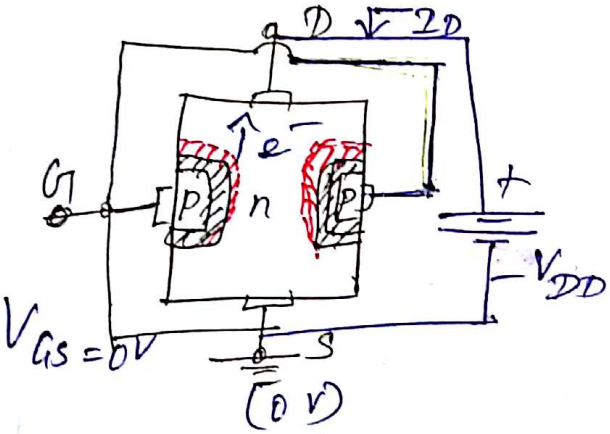
* Because of this potential difference the free electrons in n-channel is drifted towards Drain terminal so current flow in opposite direction "I_D"

* By control the potential difference between gate and source (V_{GS}), can control the width of depletion layer, so current I_D is also controlled, JFET is a voltage controlled device.

working of JFET:-

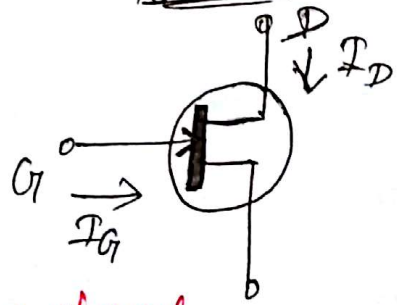
case (i)	$V_{GS}=0V$	$V_{DS}>0V$
case (ii)	$V_{GS}<0V$	

* $V_{GS}=0V \Rightarrow$ means potential at gate & source is equal, so connect gate & source terminal and source connected to zero volt ($V_{GS}=V_G-V_S=0V$)

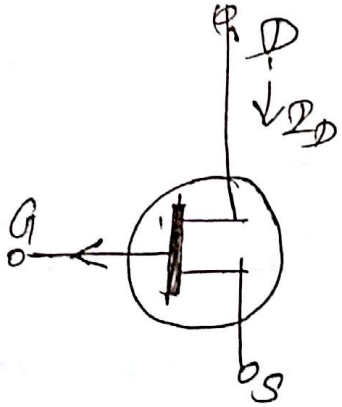


* when V_{DS} is R.B voltage depletion layer width also increases in top only.

Symbol:-



n-channel



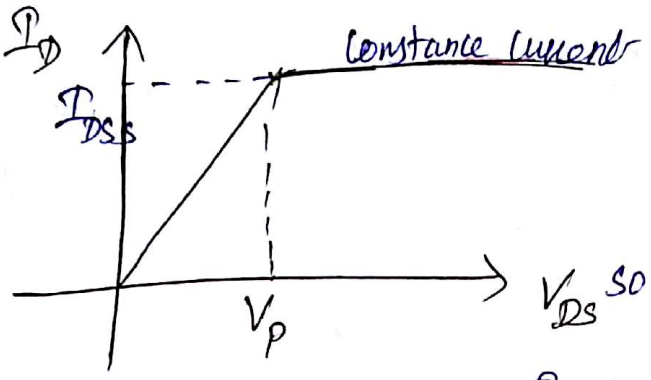
- P-channel

* Gate Current $I_G=0A$ because of that pn Junction is reverse biased

Pinch-off Voltage:-

* Increasing V_{DS}, I_D $\uparrow$es, width of depletion layer also increases

* when V_{DS} ↑ to the level, where it appears that the two depletion regions are touching each other this condition called as pinch off. - that corresponding voltage called as pinch off voltage (V_p)



* when $V_{DS} = V_p$, then Current will become Constant (I_{DSS}) so Resistance also constant.

* After V_p resistance equal to ∞ because

Slope = 0, $R = 1/\text{slope}$

* I_{DSS} ⇒ Max Drain Current ($V_{GS} = 0V, V_{DS} \geq |V_p|$)

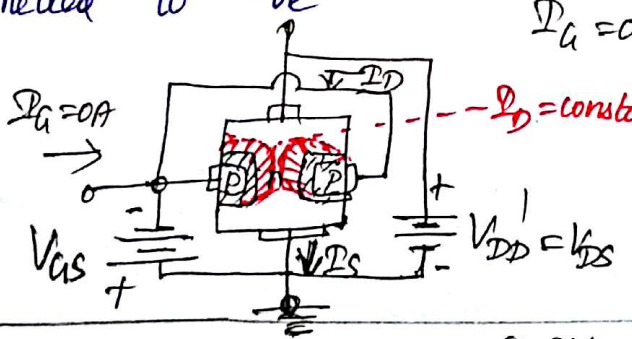
Drain source shorts circuited because ($V_{GS} = 0V$)

V_{GS} = negavetive $V_{GS} < 0V$, $V_{DS} = V_{DD} < V_{DD}$

to obtain saturation at lower value of V_{DS}

$I_D \neq I_{DSS}$ because $I_D = I_{DSS}$ is only at $V_{GS} = 0V$

For V_{DS} is Smaller V_{GS} should be Very Small (-Ve) to get some width of depletion layer, so gate terminal connected to -Ve



$I_G = 0A$ because of Reverse bias pn Junction

R.B ⇒ W ↑es. ⇒ So two region touches each other This is pinch off condition

correspond V_{DS} = pinch off Voltage

* Pinch off voltage in case (i) is more than case (ii) because gate is connected to -ve bias.

* ↑es in V_{DS}, beyond V_p I_D will remain constant this is called saturation condition

Output Characteristics of JFET:-

* I_D V_S V_{DS} ⇒ Drain to source Voltage (or) o/p voltage

Drain or o/p current

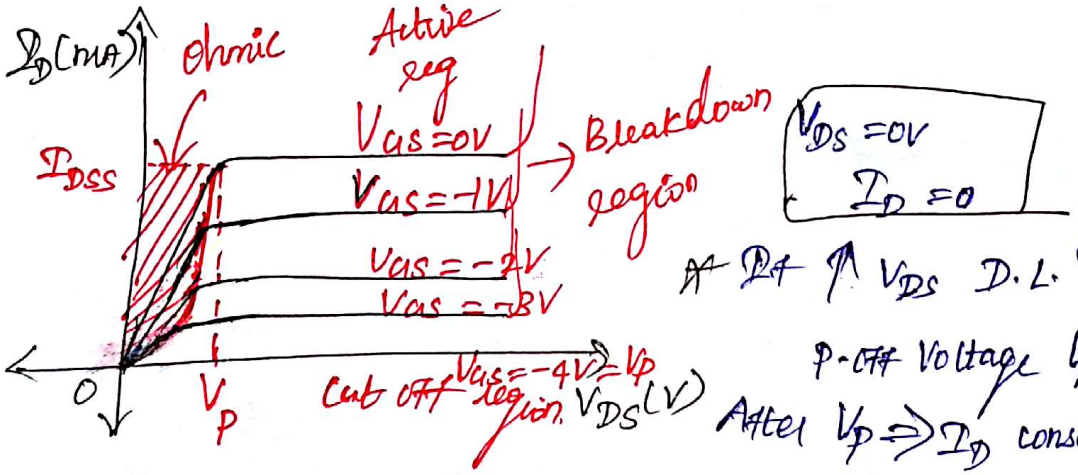
for diff V_{GS} ⇒ i/p Voltage

controlling Voltage

In n-channel $V_{GS} < 0V$

In p-channel $V_{GS} > 0V$

$I_D = I_{DSS}$ { $V_{GS} = 0V$, $V_{DS} > |V_p|$ } V_{GS}



* If ↑ V_{DS} D.L. ↑es

P-off Voltage V_p.

After V_p ⇒ I_D constant

* In case (ii) V_{GS} more -ve means it will ↑es D.L high V_p occurs very fast as lower voltage

Transfer Characteristics of JFET:-

* No linear relation b/w i/p and o/p current

$I_D = f(V_{GS})$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- I_D: o/p (or) Drain current
- I_{DSS}: Max Drain current
- V_{GS}: Gate to source voltage
- V_P: Pinch off voltage

I_{DSS} & V_P are constants

V_{GS} ⇒ control variable, because of square eqn is non linear, $V_{GS} \downarrow = I_D \uparrow$es

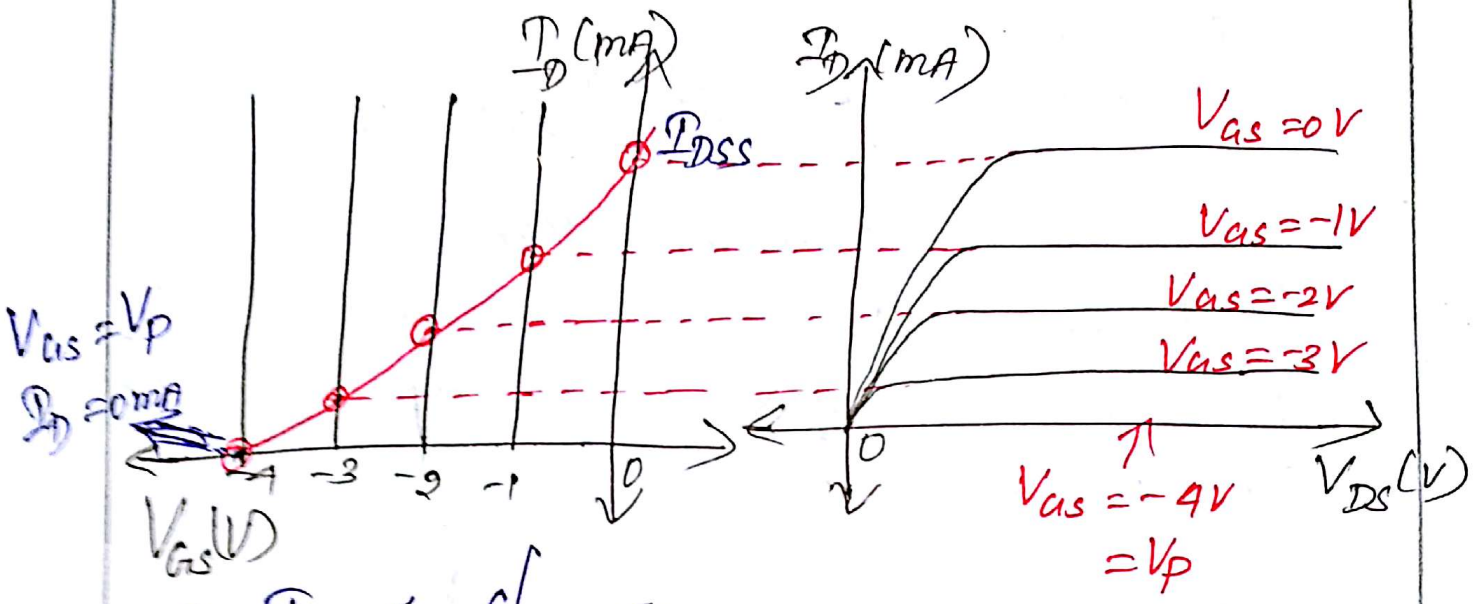


Fig:- Transfer Char of JFET

MOSFET:- Metal Oxide Semiconductor Field Effect Transistor

⇒ Like BJT and FET, MOSFET is also a active device.

* Any type of component with ability to control the flow of electron is called as active device

eg: BJT, JFET, MOSFET

* Circuit Component with no ability to control flow of electrons called as Passive device

eg: Diode, capacitor, Transformer etc....

Depletion-type MOSFET:- (N-channel D-MOSFET)

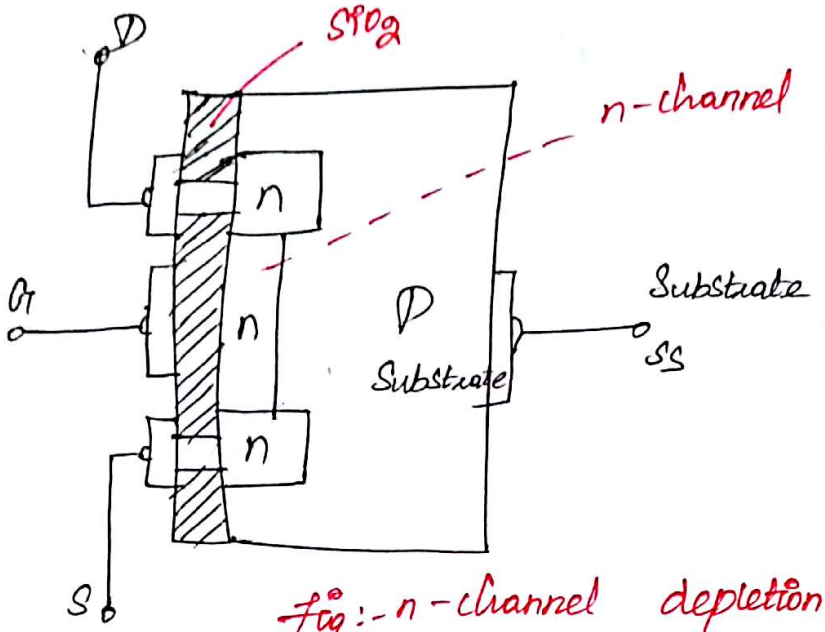


fig:- n-channel depletion-type MOSFET

* A Slab of P-type material is formed form a silicon base and it is called as Substrate.

* The Source and drain terminals are connected through metallic contacts to n-doped regions. linked by an n-channel

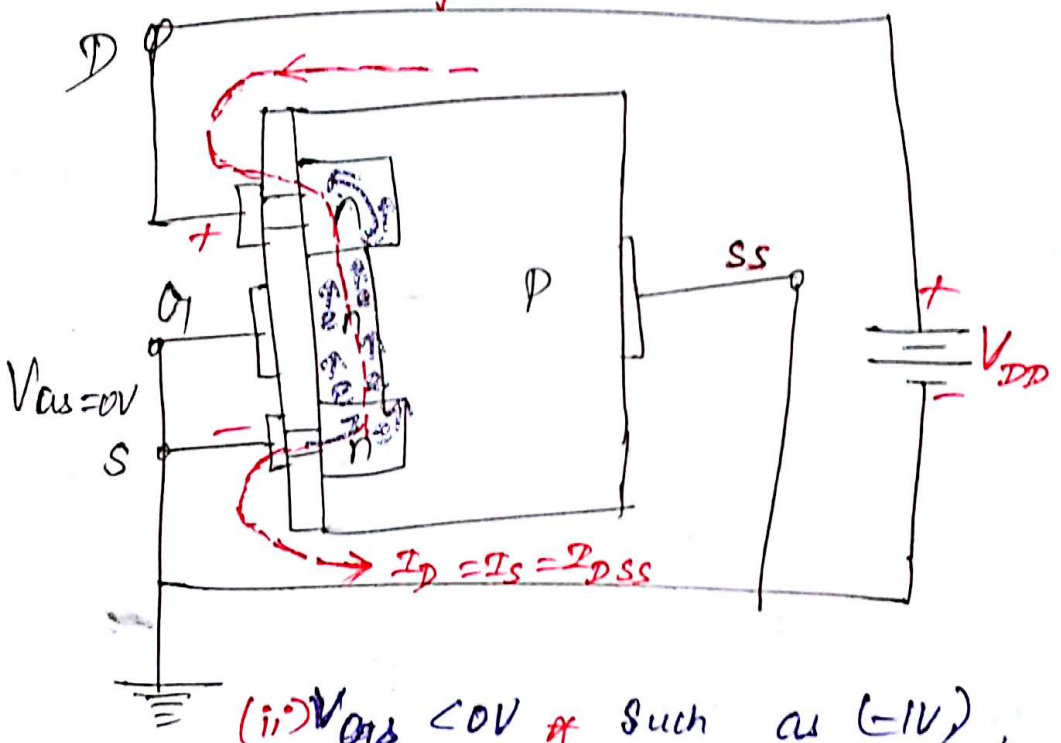
* The gate is also connected to a metal contact. Surface but remains insulated from the n-channel by a very thin SiO_2 layer. (SiO_2 layer is referred as dielectric). (D means there is no direct electrical connection b/w the gate terminal & the channel of MOSFET)

* The insulating layer between the gate and the channel has resulted is known as Insulated-gate FET, (or) IGFET

Operation and characteristics:-

(i) $V_{GS} = 0V$, If V_{DS} is applied across the drain to source terminal. The result is an attraction for the positive potential at drain by the free electrons of the n- channel and a current similar to that established through the channel of JFET.

Fig :- when $V_{GS} = 0V$ with V_{DD}



(ii) $V_{GS} < 0V$ If such as (−1V),

The negative potential at gate will tend to pressure electrons towards the P-type substrate and attract holes from the P-type substrate.

If Level of recombination between electrons and holes will occur that will reduce the number of free electrons in n-channel

* More negative bias, higher rate of recombination, resulting level of drain current, therefore reduced with rising -ve bias V_{GS}. Just like JFET.

(iii) $V_{GS} > 0V$, * the positive gate will draw additional electrons from the P-type substrate due to the reverse leakage current.

* As the gate to source voltage continues to increase in +ve direction, the drain current will increase at a rapid rate.

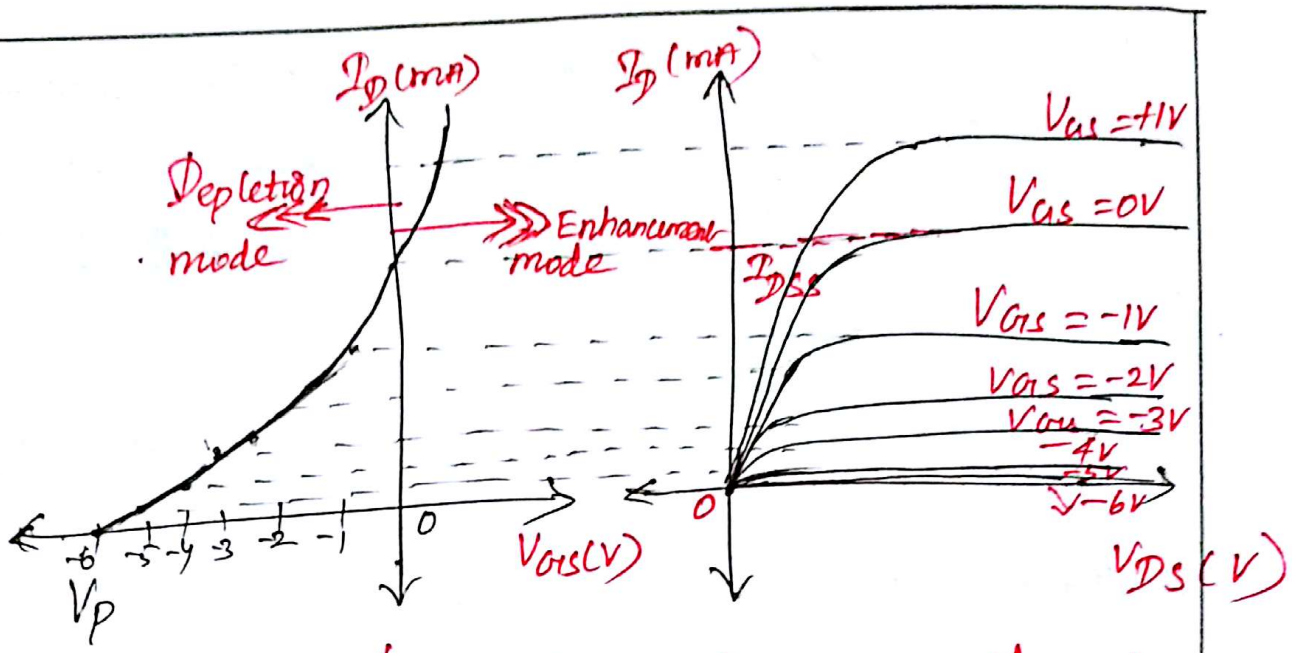
* The application of a positive V_{GS} has "enhanced" the level of free charge carriers in channel compared to $V_{GS} = 0V$.

* For this ~~region~~ reason, the region of +ve V_{GS} transfer characteristics is called as "enhancement region".

* With the region between cutoff and saturation level of I_{DSS} referred "depletion region".

by Shockley's equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Drain & Transfer Characteristics for an n-channel D-MOSFET.

Fig :-

Symbol of D-MOSFET :-

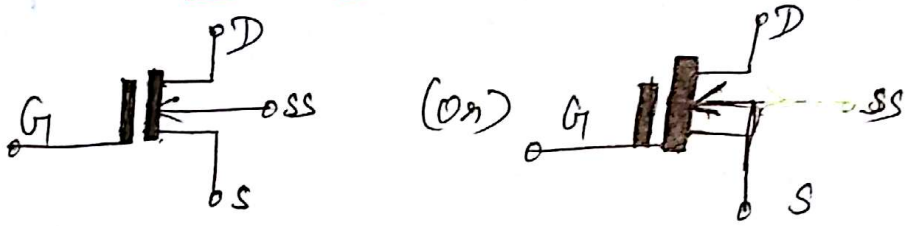


Fig :- Symbol of n-channel D-MOSFET

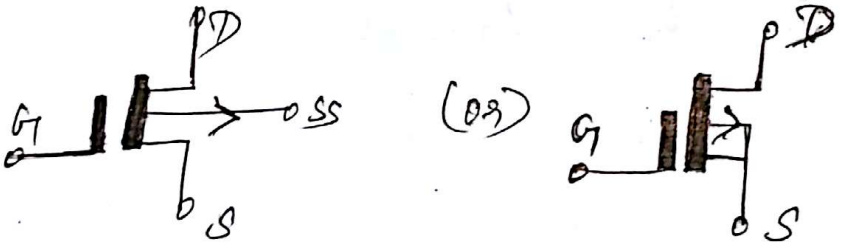


Fig :- Symbol of P-Channel D-MOSFET.

Symbol of E-MOSFET :-

Fig :- n-Channel

Fig :- P-channel

Enhancement type MOSFET (E-MOSFET):-

* Mode of operation between D-MOSFET & E-MOSFET is somewhat same, but characteristics of E-MOSFET is quite different from D-MOSFET.

* It is not defined by Shockley's equation, and drain current is now cut off until V_{GS} reaches specific magnitude.

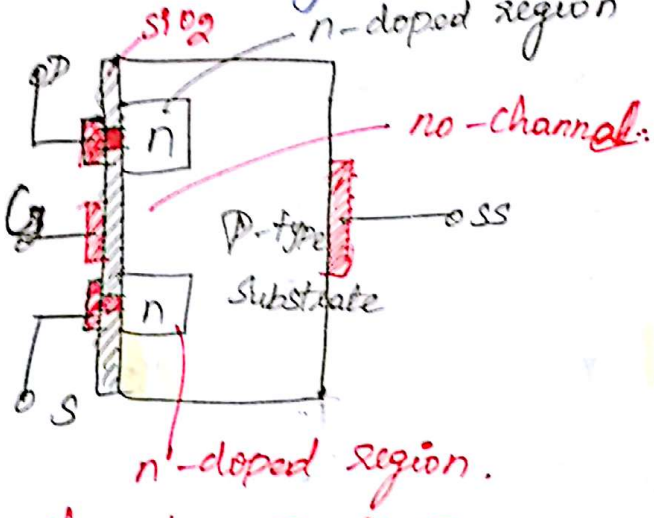


Fig:- N-Channel E-MOSFET.

* construction of E-MOSFET is same as N-channel MOSFET, but one difference is absence of a channel. (ie) Initially no-channel between two n-type doped region. (b/w D & S terminal)

Operation and Characteristics:-

i) V_{GS} is 0V & V_{DS} = 0V, the absense of an n-channel will result in a current is zero (ie) no current = 0A).

(ii) $V_{GS} = 0V$, & V_{DS} is some +ve Voltage, So there are in fact two reverse biased p-n Junctions between the n-doped regions and p-substrate to oppose any significant flow between drain and source. (no current)

(iii) $V_{GS} > 0V$ & $V_{DS} > 0V$

* +ve potential at gate will pressure the holes in the p-substrate along the edge of the SiO_2 layer.

* So electrons in p Substrate will be attracted to the positive gate and accumulate in the region near the Surface of SiO_2 region.

* The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at Gate terminal

* V_{GS} ↑es Concentration of e⁻ at SiO_2 ↑es eventually the induced n-type region support a measurable flow between drain and Source.

* The level of V_{GS} that results in significant increase in drain current is called threshold Voltage (V_T).

* The channel is non existent with $V_{GS} = 0V$ and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called "Enhancement-type MOSFET".

* For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

* when $V_{GS} > V_T$ the drain current is related to V_{GS} by,

$$I_D = k (V_{GS} - V_T)^2$$

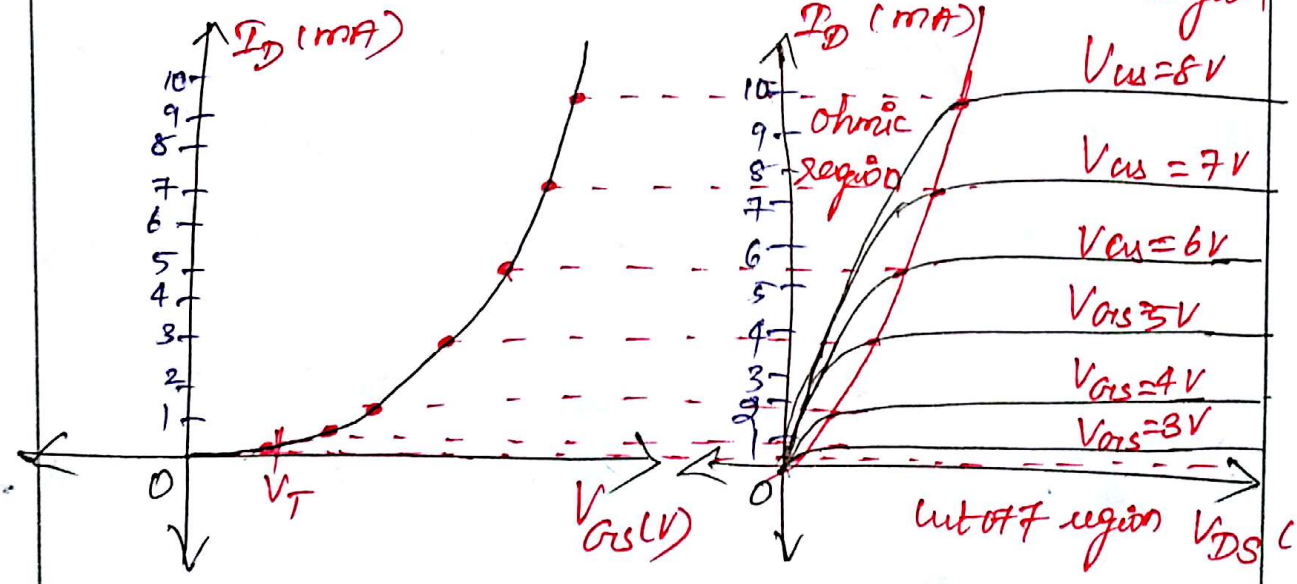


Fig:- Transfer characteristics Fig:- Drain characteristics

for n-channel E-MOSFET

CMOS :- Complementary MOSFET :-

* Construction of a p-channel and n-channel MOSFET on the same substrate, this configuration is referred to as complementary MOSFET (CMOS)

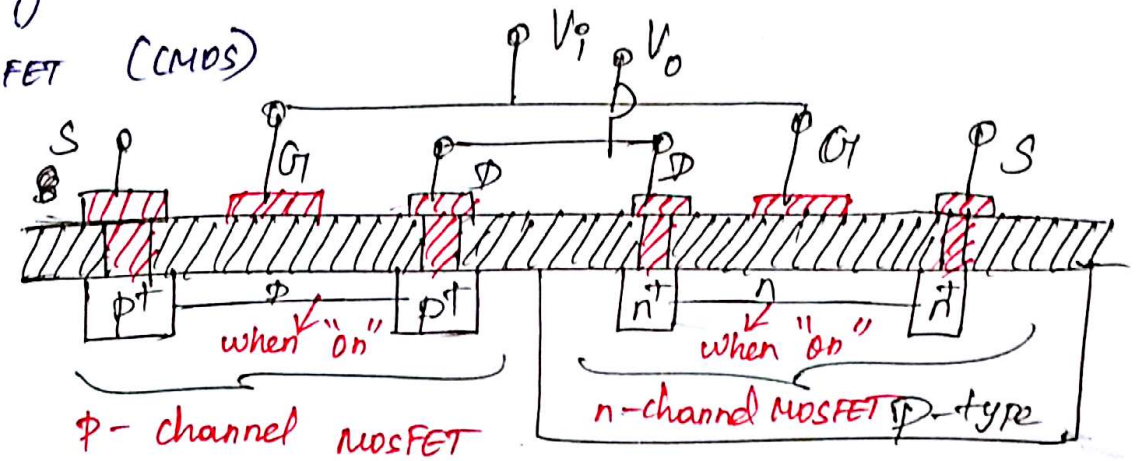


Fig:- CMOS with the connections.

* Use of complementary arrangement is as an inverter, for switching transistors, an inverter is a logic element that inverts the applied signal.

* If logic level of operations are 0V and 5V, then If i/p 0V ⇒ 5V o/p vice versa.

* Both gates are connected to applied signal and both drain are to the Output V_o. The source of p-channel MOSFET (Q_2) is connected to applied Voltage V_{SS} & in n-channel connected to ground

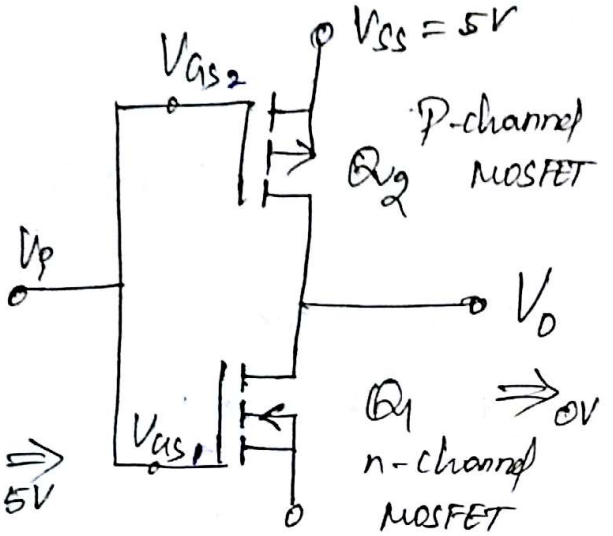


Fig:- CMOS Inverter

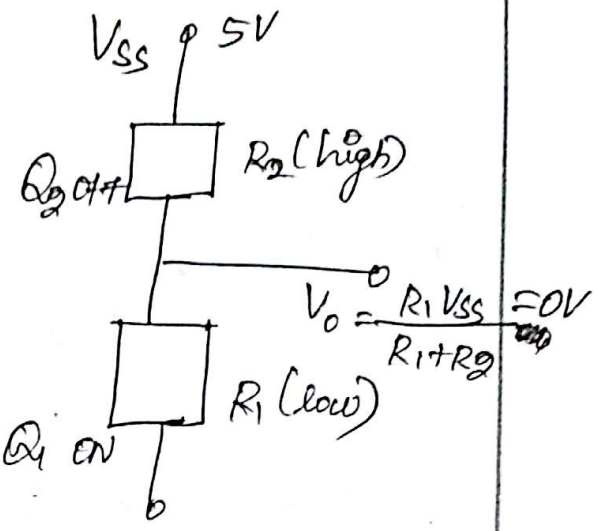


Fig:- Relative resistance levels for $V_i = 5V$

* The application of 5V at i/p should result in 0V at o/p. With 5V at V_i, $V_{GS_1} = V_i$ and Q_1 is "on" resulting in relatively low resistance between drain & source.

* Since V_i & V_{SS} are at 5V, $V_{GS_2} = 0V$, which is less than the required V_T, result is "OFF" state, so resulting resistance level b/w drain & source is quite high for Q_2.

* For $V_i = 0V$, $V_{GS_1} = 0V$, Q_1 will be "OFF" $V_{SS_2} = -5V$, turning on the P-channel MOSFET, so Q_2 will have small resistance, Q_1 will have high resistance $V_o = V_{SS} = 5V$

Breakdown Mechanism in BJT:-

* Two types of Breakdown mechanism in BJT,
  * Avalanche Multiplication.
  * Reach through (Punch through)

Avalanche Multiplication:-

When the reverse bias applied across CB avalanche breakdown occurs due to impact ionization. (Same as PN Junction diode) Electron-hole pair is generated in the collector because of high kinetic energy. There will unlimited increase of current in collector this cause BJT to breakdown.

Reach through (Punch through):-

Depletion region increases., if reverse bias across C-B increased. It Penetrates more lightly doped region. Base is lightly doped region. So the depletion region Penetrates more into base region. The base width becomes narrower. If reverse bias is Incd, depletion region spread completely across base to reach emitter this is known as reach through (or) Punch through. If V_{BE} Incs $\Rightarrow$ large current $\Rightarrow$ Breakdown occurs.

Transistor Amplifying action:-

* The input signal may be a current signal, voltage signal or a Power signal.
* An amplifier will amplify the signal without changing its characteristics.

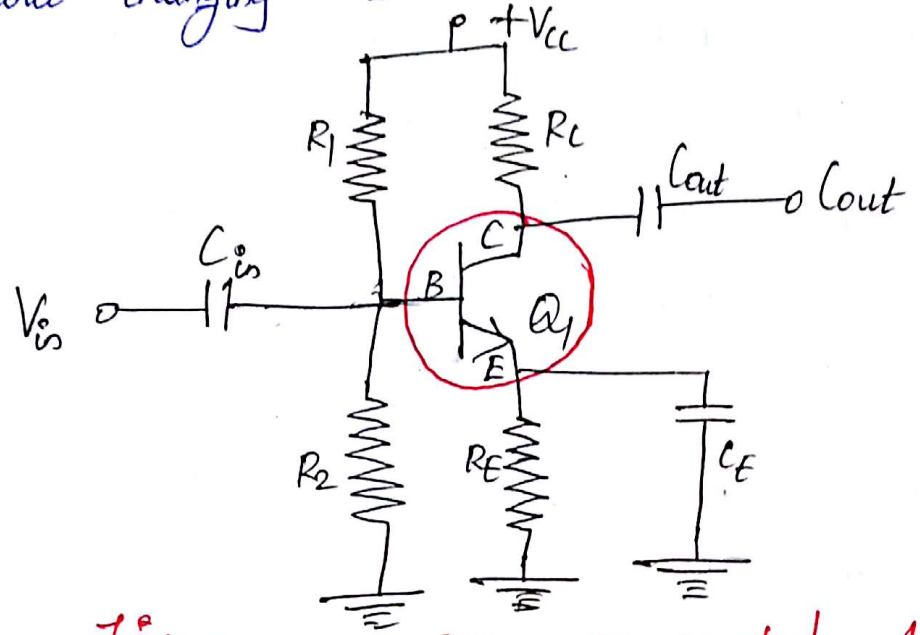


fig:- common Emitter RC coupled Amplifier.

* It is an elementary amplifier Circuit
* The main Purpose → Pre amplification.
  ⇒ To make weak signal to be Strong signals
* Cin at the i/p acts as a filter ⇒ It blocks DC and allows only AC Voltage
* R1 & R2 ⇒ Provide Proper biasing to the transistor.
  (Provides necessary base voltage to drive the transistor in "Active region"

⇒ Transistor acts as an amplifier at Active region

Active region ⇒ region b/w Cutoff & Saturation region

i.e. J_1 (EB) Emitter base in FB ⇒ Forward bias

J_2 (CB) collector Base in RB ⇒ Reverse Bias

* R_C ⇒ collector resistor R_E ⇒ emitter resistor.

↓ ⇓

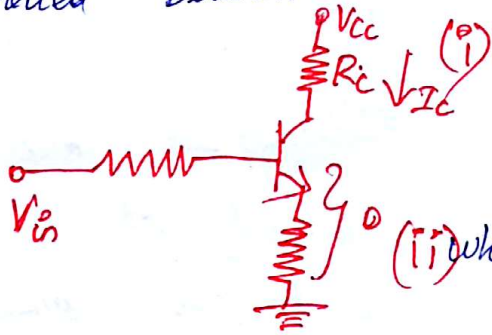
Selected in such a way that both should drop V_{CC} by 50% in the above circuit

* The C_E & R_E makes a negative feedback for making the circuit operation more stable.

* CE Configuration :- is commonly used in the audio amplifier application, because it has high gain, i.e. more than unity.

Transistor Switches :- (Transistor Inverter)

* A Suitably biased transistor functions as a switch connected between collector and emitter.



(i) when the transistor in Saturation region

i.e. J_1 ⇒ EB ⇒ F.B

J_2 ⇒ CB ⇒ R.B } ON switch

(ii) when Transistor is cut off region

i.e. J_1 ⇒ EB ⇒ R.B

J_2 ⇒ CB ⇒ F.B } OFF switch

* when i/p high voltage is applied @ base terminal, I_B ↑es, ⇒ I_C ↑es so

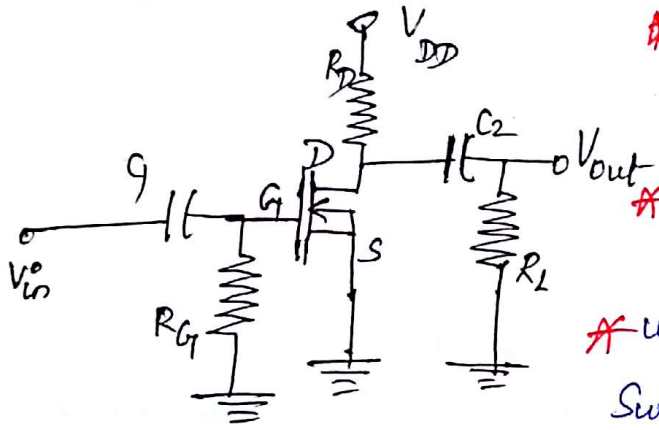
$$V_{CC} - I_C R_C = 0.$$

* when i/p low is applied · I_B ↓es ⇒ I_C ↓es

(ie) $V_{CC} = V_{CE}$ (ie $I_C = 0$)

FET as an amplifier :-

Common source DMOSFE amplifier :-



* Input signal V_{in} is coupled to the gate terminal.
* In the absence of the signal, $V_{GS} = 0$.
* when V_{in} is applied, V_{GS} swings above & below its zero value producing a variation in it drain current I_D.
* A small change in gate voltage produces a large change in drain current. This fact makes "JFET as as Amplifier"

1) During +ve half cycle of i/p s/l, -ve voltage on gate increases & produces "Enhancement mode", this increases the channel conductivity and drain current

2) During -ve half cycle of i/p s/l, the +ve voltage on gate decreases & produces "Depletion mode"

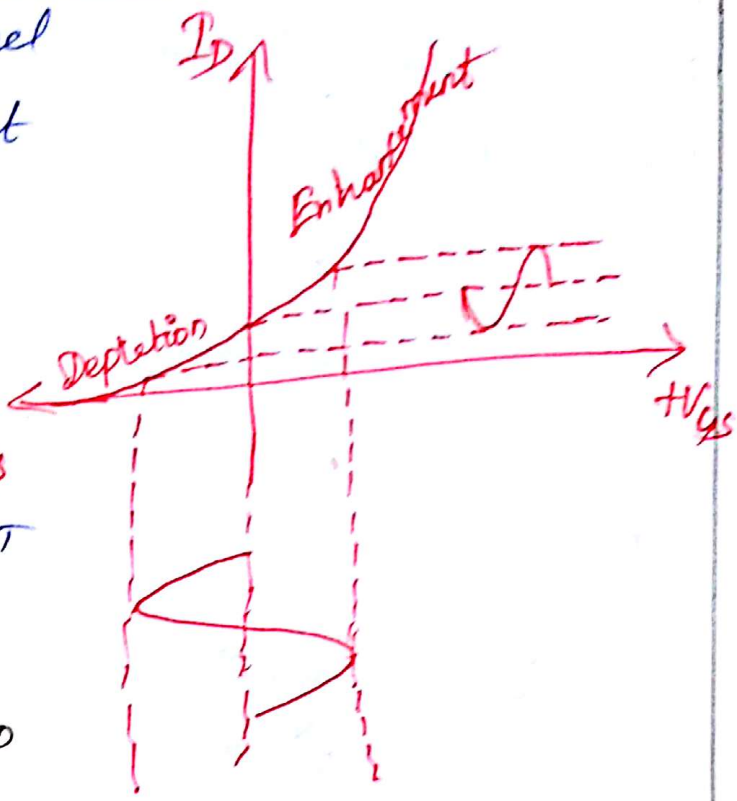
this decreases the channel conductivity & drain current

* Variation in drain current produces large AC o/p voltage across resistance R_D.

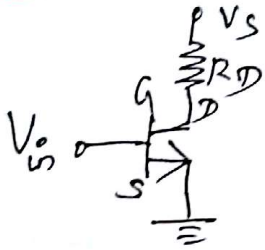
* In this way DMOSFET acts as an amplifier.

Voltage gain, $A_V = g_m R_D$

$\text{Gain} = \frac{V_{out}}{V_{in}}$



MOSFET as a Switch :-



* Required to function as switches, they should be biased in such a way that they acts between cut off & Saturation region

* cut off ⇒ no current flow ⇒ OFF Stage

* Saturation ⇒ ON Stage

1) $V_{in} = 0$, $V_{GS} = 0 \Rightarrow I_D = 0$

$I_D = 0$ $\quad I_D R_D = 0$. $\quad V_{DS} = V_S$

2) $V_{in} = +ve$, $V_{GS} = +ve$ Value

$I_D \uparrow_{es} \Rightarrow I_D R_D \uparrow_{es}$ $\quad V_S - \underbrace{I_D R_D}_{\simeq V_S} = 0$