// SELETRX) SEM IV (CR) May 2013
DSD-II

14/5/2013

Con. 6508–13. **GS–6987**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.

(2) Solve any **four** questions out of remaining **six** questions.

(3) Write the assumptions **clearly** if any.

1. (a) Identify the equivalent states in the following states table and reduce the table : **5**

Present state	Next state/output	
	input x = 0	x = 1
A	A/O	B/O
B	A/O	D/1
C	C/O	E/O
D	E/O	F/1
E	C/O	D/1
F	A/O	B/1

(b) Write VHDL Code for ~~4:1~~ 4:2 multiplexer using conditional signal assignment statements. **5**

(c) It is required that one out of 8 LED's should be glowing one after the other at regular interval. The sequence should be repeated continuously. Draw the block diagram of this circuit. and explain the function of each block in brief. **5**

(d) Name the different types of programmable devices used for digital system design. Discuss the advantages of using programmable devices. **5**

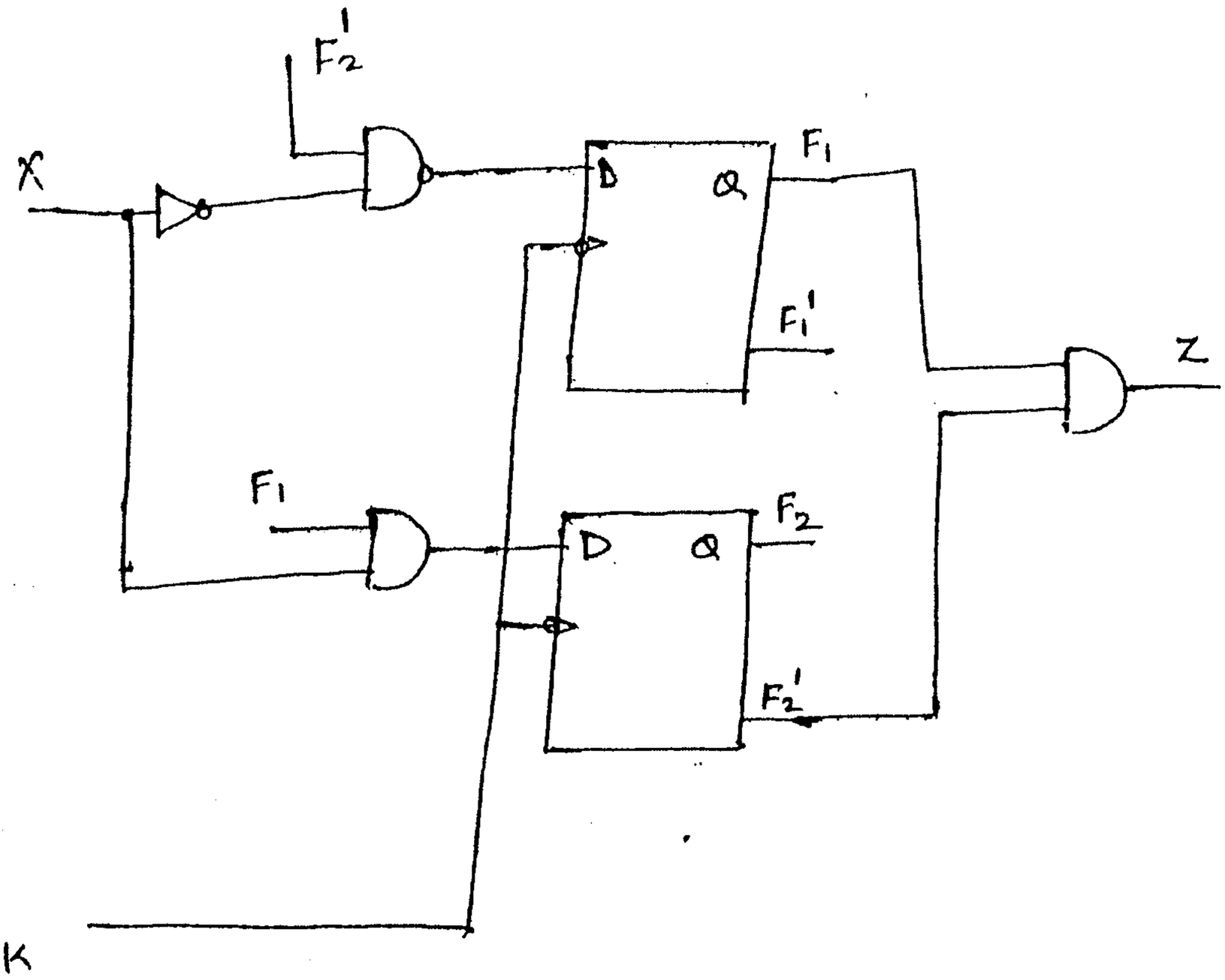
2. (a) For the sequential state machine given below :— **10**

(i) Derive the excitation and output equation

(ii) Write the next state equation

(iii) Construct state transition table

(iv) Draw the state diagram.



(b) Write a VHDL Code for a sequence detector which detects the sequence 1–0–1–1–0. **10**
Design Mealy type of machine with overlapping allowed.

3. (a) With suitable examples explain the Moore and Mealy types of sequential circuits. **6**
Compare the two types.

(b) Compare static RAM with dynamic RAM. **4**

(c) Design a 4 bit register using D flip-flops to operate as indicated in the table below :— **10**

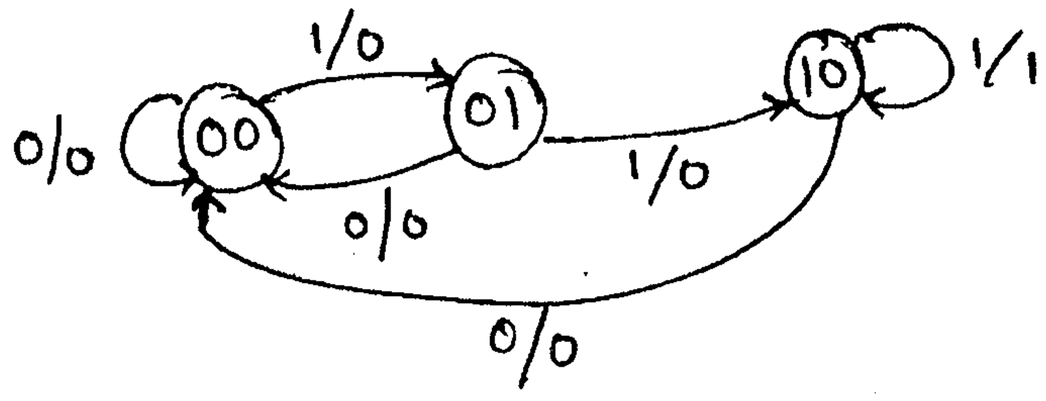
Mode	**Select**	**Operation**
a_1	a_0	
0	0	Hold
0	1	Clear
1	0	Complement the contents
1	1	Circular right shift

4. (a) Write the features of counter IC 74163. Design Mod 200 counter using the same IC. **10**

   (b) Draw the state diagram for a sequential state machine which has two inputs EN and S. As long as EN is negated (= 0), the machine should remain in reset state with output z = 0. When EN is asserted (= 1) and at S, two consecutive 0's and two consecutive 1's are received irrespective of the sequence (i.e. 0011 or 1100), the output should become 1 and remain 1 until EN is again negated ? **10**

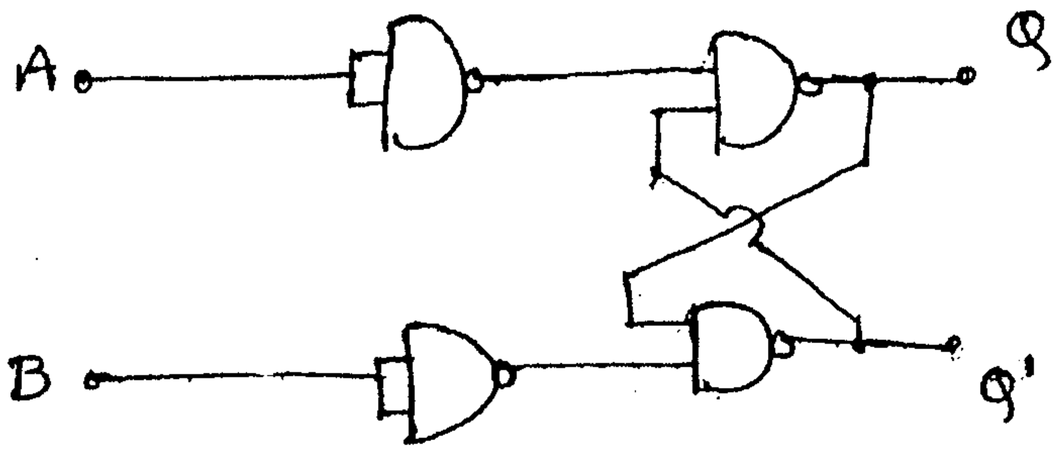
   Also draw the state table for the same.

5. (a) A sequential circuit having one input and 1 output has state diagram shown below. **10**
   Design the circuit using J.K. flip-flop.



   (b) Draw the architecture of FPGA 4000 family. Explain the function of each block. **10**

6. (a) Analyse the following feedback sequential machine :— **10**



   (b) Write a VHDL code for 8 bit barrel shifter. **10**

7. Write notes on the following :—

   (a) Fundamenal and pulse mode asynchronous sequential circuits **6**

   (b) Features of VHDL **7**

   (c) Read only memory. **7**