Code No. 3163

## FACULTY OF INFORMATICS

### B.E. 4/4 (IT) I-Semester (Supplementary) Examination, June/July 2011

### VLSI DESIGN

Time : Three Hours] [Maximum Marks : 75

Answer **ALL** questions from Part A. Answer any **FIVE** questions from Part B.

### PART—A (Marks : 25)

1. What is Threshold Voltage Loss ? 2
2. Sketch nFET-pFET pair to make a CMOS Transmission Gate. Explain the bi-directional switching ability of Transmission Gate. 3
3. Define Device Transconductance. 2
4. Sketch a circuit using CMOS complementary pair to realize a NOT gate and show a corresponding sketch giving Layer Pattern for silicon implementation. 3
5. Illustrate Lambda Design Rules. 2
6. Explain how Propagation Delay is estimated for an Inverter Switching Case. 3
7. Write two salient features and two drawbacks of Complementary Pass-Transistor Logic (CPL) approach. 2
8. Sketch a neat logic gate diagram of a Programmable Logic Array (PLA). 3
9. Sketch a 4-input AOI circuit and write verilog module for the same. 3
10. Explain how a basic clock stabilization network works. 2

### PART—B (Marks : 50)

11. (a) Explain switching action of an nFET and a pFET. 4

    (b) An n-channel MOSFET has a mobility value of $\mu_n = 560$ cm$^2$/V-sec and uses a gate oxide with a thickness of $t_{ox} = 90 \times 10^{-8}$ cm. The gate voltage is given as $V_G = 2{\cdot}5$ V, and the threshold voltage is 0·65 V.

    (i) Calculate the value of $C_{OX}$ in units of F/cm$^2$.

    (ii) Find the process transconductance.

    (iii) Find the device transconductance, if the FET has a channel length of 0·25 μm and a channel width of 2 μm. 6



(Contd.)

12. (a) Sketch and explain layers used to create a MOSFET. 4

(b) List masking sequence and explain each briefly. 6

13. Describe CMOS Process Flow using appropriate illustrative diagrams. 10

14. (a) Explain Write, Hold and Read operations in a 1 transistor DRAM cell. 6

(b) (i) Find the final voltage during a logic 1 read operation on a DRAM cell with storage capacitance, $C_s$ = 50 fF and a bit line capacitance, $C_{bit} = 8C_s$. Assume maximum voltage of $V_s = V_{max}$ = 2·5 V on the storage capacitor.

(ii) Find the hold time, given leakage current, $I_L$ = 1 nA, storage capacitance, $C_s$ = 50 fF and change in voltage across capacitor, $\Delta V$ = 1 V. 2+2

15. (a) What is Behavioral Modeling ? Explain. 6

(b) Write a behavioral description of a positive-edge-triggered D-type flip-flop using verilog. 4

16. (a) Write nFET current-voltage equations and explain briefly.

(b) State the problem of latchup and explain its prevention.

(c) Present a RC switch model for a CMOS inverter. 10

17. (a) Explain DC characteristics of a CMOS inverter.

(b) Discuss issues in Floor Planning and Routing.

(c) Write an overview of testing CMOS circuits. 10