M 22528

Reg. No. : .....

Name : .....

V Semester B.Tech. (Including Part-Time) Degree (Reg./Sup./Imp.) Examination, November 2012
(2007 Admn. Onwards)
PT 2K6/2K6 EC 504 : Computer Organization and Architecture

Time: 3 Hours Max. Marks: 100

PART – A

Answer **all** questions.

1. a) With a neat diagram explain the operational details of processor and its interconnection with memory.
   b) What is stack ? Explain the effect of operations performed on a stack with example.
   c) Explain the control sequence for executing the instruction add.
   d) Explain the notion of wide branch addressing.
   e) What is virtual memory ?
   f) Differentiate between primary and secondary memory.
   g) Explain the I/O interface for an input device.
   h) What is dairy chaining ? Explain how devices are connected to form a daily chain. **(8×5=40)**

PART – B

Answer **any one** question from the **two** choices given :

2. Explain the different addressing modes through which the operands of an instruction are specified. **15**

OR

3. a) Explain Booth's multiplication algorithm. **7**
   b) Illustrate restoring integer division algorithm with example. **8**

P.T.O.

4. a) What do you mean by micro instruction ? Explain sequencing with next address field. **8**

   b) Explain instruction execution cycle with the help of an example. **7**

   OR

5. a) Explain how control signals are generated using hardwire control unit. **8**

   b) Explain the basic organization of a microprogrammed control unit. **7**

6. What are static and dynamic memories ? **4**

   Explain how static and dynamic memory cells are implemented. Describe its working also. **11**

   OR

7. a) Explain any one cache mapping techniques in detail. **7**

   b) Explain how virtual memory address translation is performed. **8**

8. a) What are interrupts ? Explain how interrupts are serviced. **8**

   b) Explain how a parallel interface is used to connect a keyboard to a processor. **7**

   OR

9. a) Explain multiprocessor organization. **7**

   b) Compare and contrast RISC versus CISC architecture. **8**