Roll No .....

EC-605

B.E. VI Semester

Examination, June 2016

VLSI Circuits and Systems

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) What is Antifuse, define.
   b) What do you mean by well rules?
   c) Define the term locality with respect to VLSI design.
   d) Explain the various steps of VLSI design flow.

   OR

   What are the basic layout design rules?

2. a) What do you mean by sequential machines?
   b) Define pulsed latches.
   c) Differentiate between Mealy and Moore models.
   d) Explain in detail about Moore machine. State table and transition diagram with suitable diagram.

   OR

   What are the timing conditions for proper operation of combinational circuit?

3. a) Define the asynchronous machine.
   b) How asynchronous machine is different from synchronous machine explain in brief.
   c) Differentiate between fundamental mode and pulse mode asynchronous sequential machines.
   d) Illustrate the secondary state assignments in asynchronous sequential machine.

   OR

   Explain the races and hazards in asynchronous sequential machine.

4. a) Define Algorithm state machine.
   b) What are the main blocks of an ASM chart?
   c) Differentiate between hardware and firmware.
   d) What are the steps should be followed while constructing an ASM chart?

   OR

   Focus your comments on controllers and data system designing.

5. a) Define fault detection.
   b) Define PROM in brief.
   c) What are different types of faults?
   d) Describe the fault detection using Boolean difference and path sensitization method.

   OR

   Differentiate between CPLD and FPGA.

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