10/12/13 S.E. COMP Sem-III CBGS
Digital Logic design and Analysis

Con. 8955-13. **GX-12152**

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions from the remaining.
(3) **All** questions carry **equal** marks–**(20)**
(4) **Figures** to the **right** indicate **Marks**.
(5) Assume suitable data if required.

1. (a) State De-morgan's Theorems. Convert the following $(761.514)_8$ to binary and hexadecimal **5**
   (b) Subtract the following using method given below: **5**
   (i) $(11)_{10} - (22)_{10}$ using 2's complement.
   (ii) $(33)_{10} - (44)_{10}$ using one's complement.
   (c) Write short note on Ring Counter using 'D' FF. **5**
   (d) Compare FPGA and CPLD. **5**

2. (a) Perform the following directly without converting to any other base. **5**
   (i) $(63)_8 * (21)_8$
   (ii) $(D9)_H - (80)_H$
   (b) (i) Simplify the Boolean expression **5**
   $Y = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$
   (ii) Express it is standard POS Form
   $Y = (A + B)(A + C)(B + \overline{C})$
   (c) Simplify the logic function using k-map **5**
   $f(A, B, C, D) = \sum m(4, 5, 6, 7, 8, 10, 12) + d(2, 9, 11)$
   Draw the logic diagram using NAND gates only.
   (d) Explain Astable multivibrator using op-amp with neat waveforms. **5**

3. (a) Design a sequence generator to generate the sequence using 'D' FF 1101001 and repeat. Draw neat state diagram and ckt.diagram. **10**
   (b) Implement the following logic function using all 4:1 multiplexers with select inputs as 'B', 'C', 'D', 'E' only **10**
   $F(A, B, C, D, E) = \sum m(0, 1, 2, 3, 6, 8, 9, 10, 13, 15, 17, 20, 24, 30)$

4. (a) Explain 3 bit Bidirectional shift register using JK Flip Flop. Draw the neat waveforms. **10**
   (b) What is FPGA. Explain basic architecture. What are its advantages over CPLD. **10**

5. (a) Design Full adder using 3:8 decoder with active low outputs and NAND gates. **5**
   (b) Use Quine Mc-Cluskey method to simplify the logic function as given below. **15**
   $F(A, B, C, D, E) = \sum m(0, 1, 8, 10, 11, 12, 20, 21, 30) + d(14, 19)$
   Realize the above function using NAND gates.

6. (a) Design mod-10 synchronous counter using JK Flip Flops. Check for the lock out conditon. If so, how the lock-out condition can be avoided? Draw the neat state diagram and circuit diagram with Flip Flops. **15**
   (b) Explain the transfer characteristics of TTL NAND gate and hence define Fan-in and Fan out. **5**
