

Con. 3048-11.

RK-1863

(3 Hours)

[Total Marks : 100

- N.B. :** (1) Question No. 1 is compulsory.
 (2) Solve any four from Q. No. 2 to Q. No. 7.
 (3) Assume suitable data if necessary.

- | | | |
|--------|--|----|
| 1. (a) | Explain basic structure of VHDL file. | 20 |
| (b) | Compare Moore and Mealy models. | |
| (c) | Explain Universal Shift Register for four bits. | |
| (d) | Memory Organisation and Operation. | |
| 2. (a) | Explain VHDL statements. | 10 |
| (b) | What are modeling styles in VHDL and write code for full adder using component modeling. | 10 |
| 3. (a) | Write VHDL code for multiplexer IC 74151 | 10 |
| (b) | Write a code Behavioral description of simple floating point encoder. | 10 |
| 4. (a) | Explain state reduction and state Assignments techniques. | 10 |
| (b) | Design sequential circuit for detecting and overlapping sequence 1101 using J.K./F.F. | 10 |
| 5. (a) | Design a asynchronous counter using J.K./F.F. which runs through the sequences. | 10 |
| | | |
| (b) | Write VHDL code for two digit BCD counter. | 10 |
| 6. (a) | Explain Internal organization of RAM | 10 |
| (b) | Explain XC9500 Architecture. | 10 |
| 7. (a) | Explain pulsed mode Asynchronous Circuit. | 10 |
| (b) | Write short notes on :— | 10 |
| | (i) Hazards | |
| | (ii) Race Condition Stability. | |