BE | ETRX | VII (Rev) 25/5/12
VLSI Design

Con. 3927-12. **(REVISED COURSE)** **GN–6272**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of **remaining six** questions.
(3) Draw **neat** diagrams wherever **required**.

1. (a) Compare semi-custom and full-custom design. **5**
(b) Compare Burried and Butting contacts. **5**
(c) Compare ion implantation and Diffusion. **5**
(d) Draw stick diagram for CMOS inverter. **5**

2. (a) Explain the Twin Tub process in detail **10**
(b) Explain latchup in CMOS and how to prevent it. **10**

3. (a) Calculate the threshold voltage V_{TO} at V_{SB} = 0·5V for a polysilicon gate n-channel MOS transistor, with the following parameters. **10**
Substrate doping, $N_A = 10^{16}/cm^3$
Polysilicon gate doping $N_D = 2 \times 10^{20}/cm^3$
Gate oxide thickness $T_{ox} = 500A^o$
Oxide interface fixed charge density $N_{ox} = 4 \times 10^{10}/cm^2$
(b) Explain short channel effect in MOSFET. **10**

4. (a) Draw the stick diagram and mask layout using λ based design rules for a depletion load nMOS inverter with a pullup to pulldown ratio as 4 : 1. **10**
(b) Explain various sources of power dissipation in digital CMOS circuits. **10**

5. (a) Explain constant voltage and constant field scaling in detail with their merits and demerits. **10**
(b) Write Verilog code for 1 Bit full adder and use it to design a 4 Bit full adder. **10**

6. (a) Implement the following Boolean function in CMOS logic. **10**

$$Y = \frac{\text{CMOS logic}}{C(D+E) + A \cdot B.}$$

Draw the stick diagram for the circuit.
(b) What is the need for Design Rules ? Justify. **10**

7 Write notes on (any **two**) :— **20**
(a) Wafer processing
(b) MOS capacitor
(c) VLSI design flow.
