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06ELN15/25

First / Second Semester B.E. Degree Examination, June-July 2009
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note : 1. ***Answer any Five full question, choosing at least two from each part.***
2. Answer all objectives type questions only in OMR sheet page 5 of the Answer Booklet.
3. Answer to the objective type questions on sheets other than OMR will not be valued

PART – A

1 a. i) Zener diode acts as a _____ device.
A) Constant current B) Constant voltage
C) Constant power D) Variable voltage.

ii) The barrier potential of a silicon p-n junction is approximately
A) 0.3 V B) 0.1 V C) 0.7 V D) 1.2 V.

iii) In reverse bias the diode can be represented as
A) Open circuit B) Short circuit
C) A battery of 0.7 V D) A current source with constant current.

iv) A half wave rectifier is fed from secondary of a transformer whose output voltage is 12.6 V. The DC voltage of the rectifier output is
A) 12.6 V B) 5.66 V C) 17.8 V D) 11.32 V **(04 Marks)**

b. Draw a full wave rectifier and give the expressions for i) DC voltage; ii) Ripple frequency; iii) PIV; iv) Efficiency; v) RMS value of voltage. What are its advantages over half-wave rectifier? **(08 Marks)**

c. A Zener diode has a breakdown voltage of 10 V. It is supplied from a voltage source varying between 20-40 V in series with a resistance of 820 Ω. Using an ideal Zener model obtain the minimum and maximum Zener currents. **(08 Marks)**

2 a. i) In a transistor the part heavily doped is
A) Emitter B) Base C) Collector D) All are equally doped

ii) The relation between α and β is given by
A) $\alpha = \beta$ B) $\alpha = \frac{\beta}{1-\beta}$ C) $\alpha = \frac{\beta}{1+\beta}$ D) $\alpha = \frac{1}{\beta}$

iii) In the active region the collector – Base junction is
A) Forward biased B) Reverse biased
C) Driven from Forward bias to reverse bias D) Not biased

iv) In CE configuration, when collector current is zero, VCE equals
A) $\frac{V_{CC}}{R_C + R_E}$ B) V_{CC} C) $\frac{V_{CC}}{R_C}$ D) $\frac{V_{CC}}{R_E}$ **(04 Marks)**

b. Draw the common Emitter circuit. Draw the input and output curves and explain the terms active region, cut off region and saturation region. **(08 Marks)**

c. Determine the transistor currents in the Fig.Q.2(c) if $\beta = 100$ **(08 Marks)**

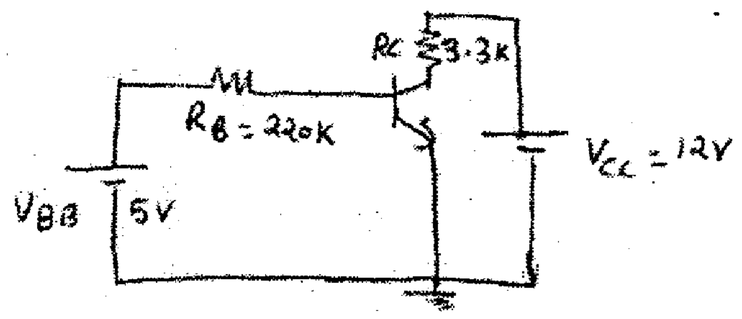


Fig.Q.2(c).

3 a. i) When used as a switch the transistor operates in
A) Active region B) Saturation and cut off C) Cut off region D) Active and saturation.

ii) When used as an amplifier the transistor operates in
A) Active region B) Saturation region C) Cut off region D) Can be in any of them

iii) Even with sinusoidal base current we get non-sinusoidal collector current in common emitter configuration because of
A) Noise introduced in base current B) Large resistance of signal source
C) Large input resistance of transistor D) Non parallel output characteristics

iv) The stability factor S is the rate of change of collector current with
A) Base current B) Reverse saturation current C) Emitter current D) VCC.
(04 Marks)

b. What is the meaning of transistor biasing? Draw a neat sketch to explain the base biasing of a transistor in CE mode. What is its stability factor S? **(08 Marks)**

c. Draw the DC load line for the voltage-divider biasing circuit shown in Fig.Q.3(c). Find the collector current and the Q point. **(08 Marks)**

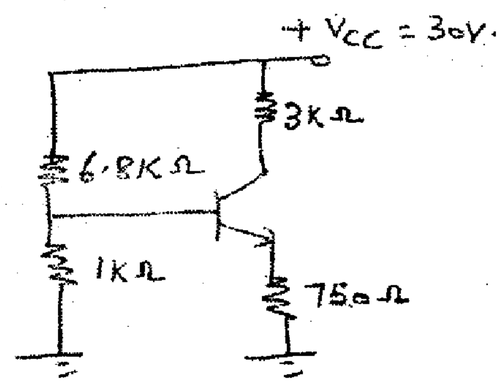


Fig.Q.3(c).

4 a. i) The SCR is a _____ device
A) NPN B) PNP C) PNPN D) PNN

ii) A relaxation oscillator uses
A) MOSFET B) SCR C) UJT D) BJT

iii) An FET is a _____ controlled device
A) Voltage B) Power C) Current D) Doping

iv) The gate current in a JFET is
A) Very large B) Very small C) Significant D) Depends on the input voltage.
(04 Marks)

b. Draw the structure and symbol of an SCR. Explain its operation and V-I characteristics. **(08 Marks)**

c. Explain the construction and working of an UJT. **(08 Marks)**

PART – B

5 a. i) The stability of an amplifier_____ with negative feedback
A) Improves B) Deteriorates
C) is not affected D) Depends on amount of negative feedback

ii) The Barkhausen criterion states that
A) $A = B$ B) $A = \frac{1}{\beta}$ C) $A\beta = 1$ D) $A\beta = 0$.

iii) In an oscillator we use _____ feedback
A) Positive B) Negative C) Neither D) Unity gain

iv) The input capacitor in a CE amplifier blocks
A) AC signal B) DC component
C) Both AC and DC D) Noise of a particular frequency **(04 Marks)**

b. Draw a neat circuit diagram of Hartley's oscillator and explain its working. What is the frequency of oscillations? **(08 Marks)**

c. Design a Colpitt's oscillator for a frequency of oscillation of 100 kHz. **(08 Marks)**

6 a. i) The op amp is basically a _____ amplifier
A) Positive feedback B) Differential
C) Common emitter D) Common – signal

ii) In an inverting amplifier, R_1 = 1K and R_f = 2K. If input voltage is 2V, output voltage is
A) –2V B) –0.5 V
C) 4V D) –4V

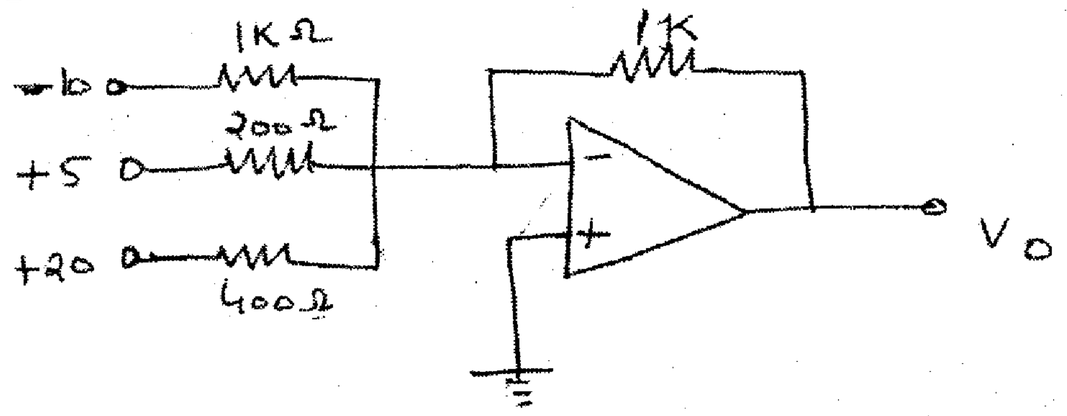
iii) The CMMR should be
A) Close to unity B) Much larger than unity
C) Zero D) Much smaller then unity

iv) When both the inputs of op amp are grounded, the voltage across the output is called
A) Output off set voltage B) Output grounded voltage
C) Output bias voltage D) Output common voltage **(04 Marks)**

b. What are characteristics of an ideal op amp? **(04 Marks)**

c. Show with a circuit diagram how the op amp can be used as an integrator. **(06 Marks)**

d. Find the output voltage for the circuit below. **(06 Marks)**



7 a. i) $(11011)_2 = (\_\_\_\_\_)_8$
A) $(33)_8$ B) $(17)_8$ C) $(25)_8$ D) $(28)_8$

ii) The 2′S complement of 1100110 is
A) 0011001 B) 0011010 C) 1100001 D) 1100010

iii) The BCD representation of decimal 10 is
A) 00001010 B) 00001001 C) 00010000 D) 10100000

iv) The binary of $(A5)_{16}$ is
A) 00100111 B) 00100101 C) 10100101 D) 10100011 **(04 Marks)**

b. Draw the block diagram of a super hetrodyne AM receiver and explain the function of each block. **(08 Marks)**

c. i) Convert $(10110011010)_2$ into octal, decimal and hexadecimal; ii) Subtract using 2′S complement $(15 - 7)_{10}$. **(08 Marks)**

8 a. i) A + AB = _____
A) AB B) A C) B D) 1 + A

ii) Universal gate is
A) NOT B) AND C) OR D) NAND

iii) If x + 1 = 1 and x . 1 = 0, then x is
A) 0 B) 1 C) Could be 0 or 1 D) Situation can never be true.

iv) The output is high only when both inputs are zero to a gate. The gate is
A) AND B) NOR C) OR D) NAND. **(04 Marks)**

b. Draw a full adder circuit with the truth table. **(06 Marks)**

c. Simplify $ABC + AB\overline{C} + \overline{A}BC$. **(04 Marks)**

d. Implement OR and AND gates using NOR gates. **(06 Marks)**

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