BTS – III – 11.13 – 1198

B. Tech. Degree III Semester Examination November 2013

EB/EC 1304 DIGITAL ELECTRONICS

(2012 Scheme)

Time : 3 Hours Maximum Marks : 100

PART A

(Answer *ALL* questions)

(8 x 5 = 40)

I. (a) (i) Perform the following conversions

$(101)_{16} = (\quad)_2 = (\quad)_8$

(ii) Find the 4-bit result using 2's complement arithmetic

$(4)_{10} - (5)_{10}$

(iii) $(89)_{10} = (\quad)_{BCD} = (\quad)_{excess\ 3}$

(iv) (1) $(1101)_{gray} = (\quad)_{binary}$

(2) $(1101)_{binary} = (\quad)_{gray}$

(b) Reduce the following expression

$F_{(A,B,C)} = ABC + A\bar{B}C + \bar{A}B\bar{C} + B\bar{C}$

(i) using Boolean theorems
(ii) using K map

(c) Design a full subtractor using basic logic gates.

(d) Design a 4 input priority encoder with the help of the truth table.

(e) Convert SR to T FF.

(f) Draw the circuit of a serial adder and explain.

(g) Define the following terms with respect to a logic gate.
(i) Propagation delay
(ii) Power dissipation
(iii) Noise margin
(iv) Fan in
(v) Fan out.

(h) Draw and explain the circuit of a tri-state inverter logic gate.

PART B

(4 x 15 = 60)

II. (a) Obtain the minimal expression using Quine-McClusky method. (10)

$F_{(A,B,C,D)} = \sum m(1,5,6,12,13,14) + d(2,4)$

(b) Convert to POS (3)

$Y_{(A,B,C)} = A\bar{C} + BC + \bar{A}\bar{B}$

(P.T.O.)

(c) Correct the error if any in the 7 bit even parity hamming code "1111110" received in the format $D_7 D_6 D_5 P_4 D_3 P_2 P_1$ (2)

OR

III. (a) Reduce using K map and realize using NAND gates only. (10)

$F_{(A,B,C,D,E)} = \sum m(2,9,13,18,19,23,25,27,29,31)$

(b) An air conditioning system in an office is turned on under any of the following conditions (3)

- If temperature (T) exceeds 78° F on weekends.
- If humidity (H) is high
- If there is at least one person in the room on week days (W)

Write the logic expression for controlling the air-conditioning unit.

(c) Implement using 2 input NOR gates only (2)

$Z = (a + \bar{b})(cd + \bar{e})$

IV. (a) Draw the logic diagram of a 4 bit carry look ahead adder and explain how this speeds up addition process (10)

(b) Design a circuit for an active low 2 to 4 decoder with an active low enable input ($\bar{E}$) (3)

(c) Realize using 4:1 multiplexer $\delta(A,B,C) = \sum m(3,4,6,7)$ (2)

OR

V. (a) Explain the BCD addition process and design a BCD adder using 4 bit binary adders. (10)

(b) Write the program table and implement using a PLA (5)

$P_{1(A,B,C)} = \sum m(0,1,3,5)$

$P_{2(A,B,C)} = \sum m(0,3,5,7)$

VI. (a) Design a 3 bit up down synchronous counter using TFFs. (10)

(b) Draw the circuit of a bit Ring/Johnson counter with mode control. Explain with the help of waveforms. (5)

OR

VII. (a) Draw and explain the circuit of a 3 bit binary multiplier. (10)

(b) Design a 3 bit asynchronous counter that counts 0-1-2-3-6-7 (3)

(c) Draw the circuit of a 3 bit PISO shift register. (2)

VIII. (a) Explain the circuit of a 2 input TTL NAND gate. (10)

(b) Compare totempole and open collector output configurations of TTL (3)

(c) Bring out the differences between (2)

(i) V_{IH} & V_{OH}

(ii) I_{IL} & I_{IH}

OR

IX. (a) Explain the different techniques for interfacing TTL to CMOS and CMOS to TTL (10)

(b) Draw and explain the circuit of CMOS inverter. (5)

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