God bless us all.

UNIT-I

POWER SEMICONDUCTOR DEVICES.

Introduction:

Power electronics is the study of electronic circuits used to convert and control the flow of electrical power

[or]

Power electronics deals with the applications of solid state electronic devices in the control and conversion of electric power.

Power Electronics embraces the studies of :-

a) Power :-

It deals with both rotating and static equipment for the generation, transmission, distribution and utilisation of vast quantities of electrical power.

b) Electronics :-

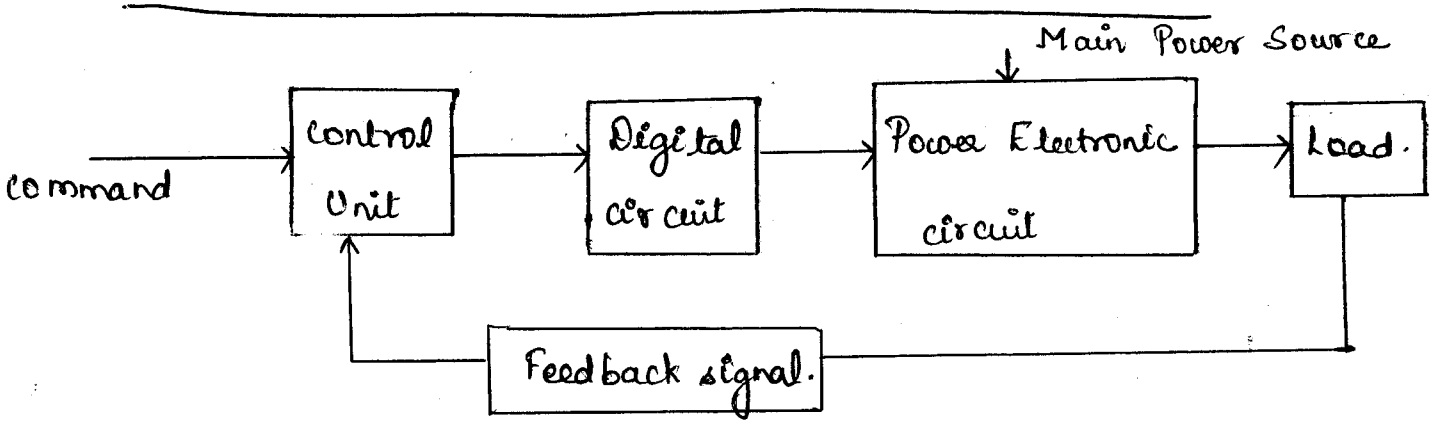
It deals with the study of semiconductor devices and circuits for the processing of information at lower power levels.

c) Control :-

It deals with the stability and response characteristics of closed loop system.

Power electronics deals with the use of electronics for control and conversion of large amounts of electrical power.

REPRESENTATION OF POWER ELECTRONIC SYSTEM.



* The main power source may be either ac or dc based on the application.

* The output of the power electronic circuit may be variable ac or dc, or it may be variable voltage and frequency, based on the requirement.

* The feedback component measures a parameter of the load (say for eg.. speed), and compares it with the command signal

* The difference between the two signals, through the digital circuit controls the instant of turn on of the semiconductor device.

* The load circuit can be controlled over a wide range with the adjustment of the command signal.

Application of power electronics:-

1. Aerospace:
   - Space shuttle power supplies
   - Satellite power supplies
   - aircraft power system.
2. commercial :-
   - Advertising, heating, air conditioning, power supplies
   - computer, office equipment, elevators, light dimmers
   - Uninterruptable power supplies, central refrigeration.
3. Industrial:
   - Arc and industrial furnaces, blowers and fans, pumps and compressors, industrial lasers, transformer tap changers, rolling mills, textile mills, excavators, cement mills, welding.
4. Residential:-
   - Air conditioning, cooking, lighting, refrigerators, electric-door openers, dryers, fans, personal computers, vacuum cleaners, washing m/c's, food mixers.
5. Telecommunication:-
   - Battery chargers, power supplies.
6. Transportation:
   - Battery chargers, traction control of electric vehicles, electric locomotives, street cars, trolley buses, subways, automotive electronics.
7. Utility systems:
   - High voltage dc transmission, excitation systems, VAR compensation, static circuit breakers, fans and boiler feed pumps, supplementary energy systems (solar, wind)

Advantages of power electronic system:-

* High efficiency due to low loss in power semiconductor devices.
* High reliability of power electronic converter system.
* Long life and less maintenance due to absence of any moving parts.
* Flexibility in operation.
* Fast dynamic response compared to electromechanical converter system.
* Small size and less weight, ∴ lower installation cost.

Disadvantages of power electronic system:-

* Circuits in power electronic system have a tendency to generate harmonics in the supply system as well as the load circuit.
* AC to DC and ac to ac converters operate at low input power factor under certain operating condition.
* Regeneration of power is difficult in power electronic converter system.
* Power electronic controllers have low overload capacity.

Power Semiconductor devices :-

S.No	Device	Voltage (V)	Current (A)	frequency.
1.	Power diodes	3000 V	3500 A	1 KHz
2.	SCR (Silicon controlled rectifier)	6000V	3500A	1KHz
3.	SITHs (Static induction thyristors)	4000 V	2200 A	20 KHz
4.	GTO's (Gate turn off thyristor)	4000V	3000 A	10 KHz
5.	MCTs (MOS controlled thyristors)	600V	60A	20KHz
6.	TRIAC	1200V	300 A	400 Hz
7.	Power BJT	1200V	400 A	10 KHz
8.	Power MOSFETs	1000V	50 A	100 KHz
9.	SITs (Static induction transistor)	1200V	300 A	100KHz
10.	IGBTs (Insulated gate bipolar transistor)	1200V	400 A	20 KHz

classification of power semiconductor devices:

1. Based on turn ON and turn OFF chs :-

a) Uncontrollable power semiconductor devices:-

DIODE : ON and OFF state are not dependant on the control signal. They depend on the power supply.

b) Partially controllable power semiconductor devices:

SCR, TRIAC, DIAC : They are turned ON by gate signal, but they are turned OFF by load (or) line signal (commutation)

c) Fully controllable power semiconductor device:

Power BJT, MOSFET, IGBT, GTO : Turned ON and OFF by gate signals.

2. Based on gate signal:

a) Pulse gate requirement:

SCR, GTO, SITH, MCT : Require pulse gate to turn ON. Once they are ON gate pulse is removed.

b) Continuous gate requirement:

BJT, MOSFET, IGBT : Requires continuous signal to keep them in ON state

3. Based on current conduction capability:

a) Unidirectional current devices : SCR, GTO, BJT, MOSFET, IGBT

b) Bidirectional current device : TRIAC, RCT (Reverse conducting thyristor)

4. Based on voltage withstanding ability:

a) Unipolar voltage withstanding : BJT, MOSFET, IGBT

b) Bipolar voltage withstanding : SCR, GTO

Power Electronic Converters:-

* A power electronic system consists of one or more power electronic converters.

* A power electronic converter is made up of some power semiconductor devices controlled by integrated circuits.

1. Diode Rectifiers:-
   * It converts ac voltage to fixed dc voltage.
   * Used in battery charging, electric traction, UPS, Welding

2. Phase controlled rectifiers (AC to DC converters):-
   * They convert constant ac voltage to variable dc output voltage.
   * Used in dc drives, chemical industries, excitation system for synchronous machines.

3. DC choppers (DC to DC converters):-
   * It converts fixed dc input to controllable (variable) dc output voltage.
   * dc drives, subway cars, battery driven vehicles.

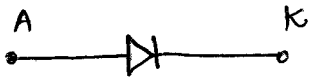
4. Inverters (DC to ac converters):-
   * It converts fixed dc voltage to a variable ac voltage.
   * Induction motor and synchronous motor drives, UPS, HVDC transmission.

5. Ac to AC converters:-
   It convert fixed ac to variable ac. They are of two types.
   (i) Ac voltage regulator:-
      * It converts fixed ac to variable ac at same frequency.
      * lighting control, speed control of fans, pumps.
   (ii) Cycloconverters:-
      * It converts input power at one frequency to output power at different frequency.
      * slow speed large ac drives like rotary kiln.

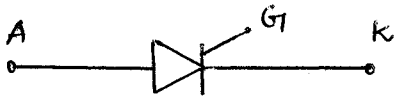
6. Static switches:-
   Power semiconductor devices can operate as static switches.

Symbols of power semiconductor devices.

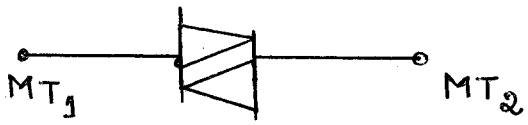
1. DIODE :



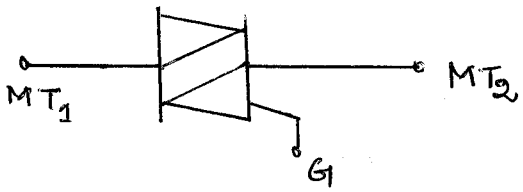
2. SCR :



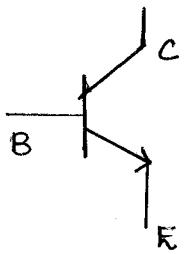
3. DIAC :



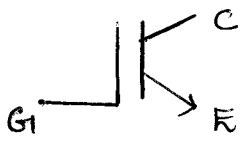
4. TRIAC :



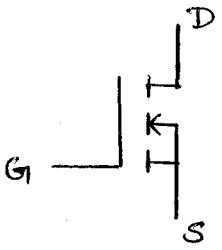
5. BJT :



6. IGBT :



7. MOSFET :



V-I CHARACTERISTICS OF POWER SEMICONDUCTOR DEVICES:

POWER DIODES:-

* It is an uncontrolled device.

* The difference between ordinary diode and power diode is that current and voltage rating are high in a power diode.

Construction:-

*A power diode is a two terminal PN junction device

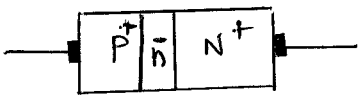
* The PN junction is formed either in Germanium or silicon by alloying, diffusion and epitaxial growth.

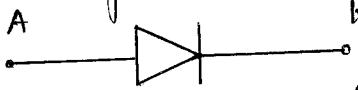
* It has two terminals namely anode and cathode.

* Anode refers to the P-type region.

* Cathode refers to the N-type region.

[Structure of power diode is slightly diffent than normal diodes. On n^+ substrate, lightly doped n^- epitaxial layer or drift region is grown]





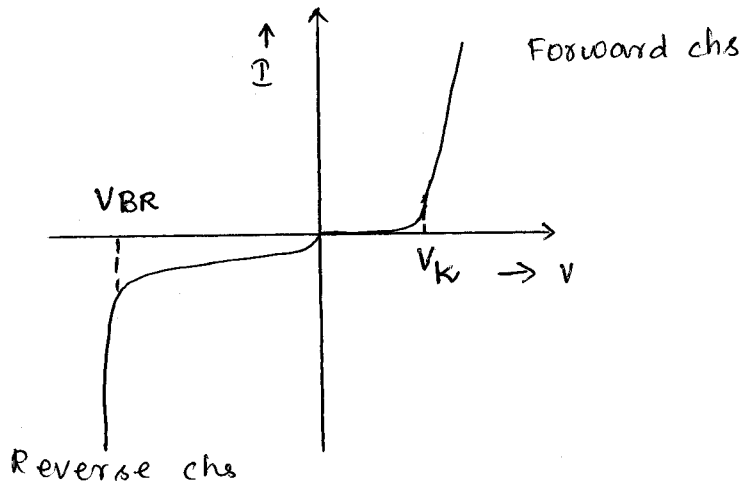
Anode Cathode.

V-I characteristics:-

* It is a graph between the voltage applied across the device and the current flowing through it.

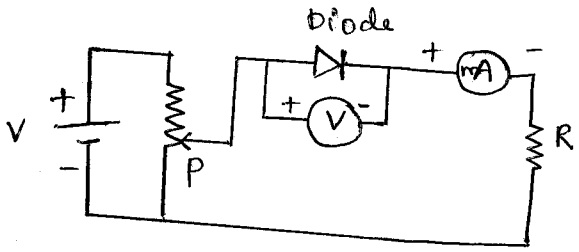
* VI characteristics may be divided into two parts namely

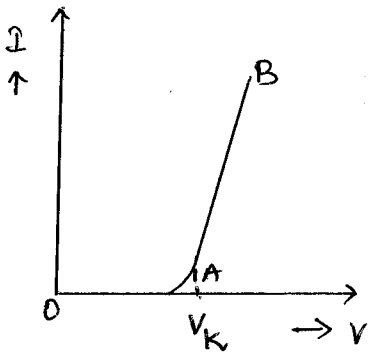
(i) Forward characteristics (ii) Reverse characteristics.



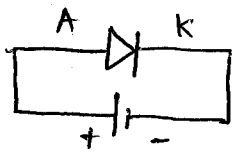
V-I CHARACTERISTICS.

Forward characteristics:





Forward characteristic.



→ forward biased.

* When anode is positive with respect to cathode, the diode is said to be forward biased.

* Now the voltage to the device is increased in steps and the corresponding values of current is noted down. A graph is plotted between Vge and current.

* A curve O AB is obtained and is known as forward characteristics.

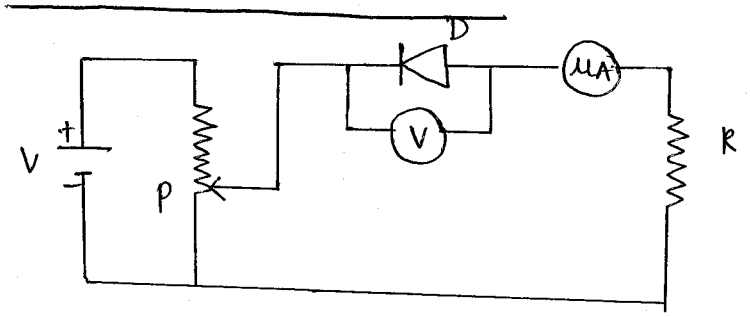
* It is seen that the current through the diode is zero till point A is reached.

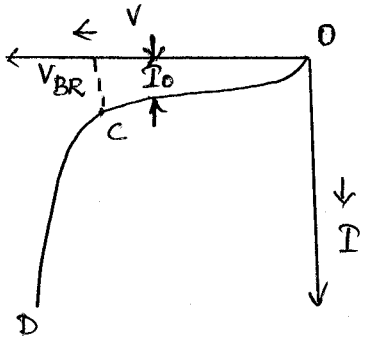
* It is because the applied voltage is opposed by the junction voltage(0.7V for Si, 0.3V for Ge)

* As the voltage is increased beyond the point A, the diode starts conducting.

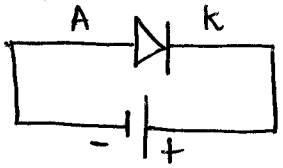
* The voltage at which the diode starts conducting is called as knee voltage (V_K) (or) barrier vge (V_B) (or) cut in voltage (V_γ) (or) threshold vge (V_{TD}).

Reverse characteristic :-





Reverse characteristics.



→ Reverse biased

* When the cathode is said to be positive with respect to the anode the diode is said to be reverse biased.

* In this condition the diode is said to be in OFF state, with very small minority carrier current flowing through it. This is called the reverse saturation current (I_O). (Constant current)

* When the reverse voltage to the diode is increased, the diode breaks down (at point C) and the current increases rapidly. (as shown by CD). This high reverse voltage is called as reverse breakdown voltage.

1. Reverse breakdown voltage (or) Peak inverse voltage (PIV) :- (V_{BR})

It is the maximum voltage the diode can withstand on reverse biased condition.

2. Maximum forward current :- ($I_{f\,max}$)

It is the maximum forward current that can be applied to the diode without damaging it.

3. Peak forward voltage ($V_{f\,max}$) :-

It is the maximum voltage drop across diode when it is forward biased.

Its value is 0.6V for ordinary diode and 2V for power diode. [$V_{f\,max}$ should be minimum to keep power loss minimum).

4. Reverse recovery time (t_{rr}) :-

It is the time taken by the current to change from ON state to OFF state.

5. Maximum reverse current :- (I_{RM})

It is the maximum current through the diode in the reverse biased condition.

Diode current equation: (Schockley diode equation)

$$I_D = I_S \left(e^{V_D/nV_T} - 1\right)$$

I_D = diode current.

$I_S = I_O$ = reverse cunt.

n = ideality factor = 1 to 2.

V_T = thermal voltage = $\frac{kT}{q}$

$k = 1.3806 \times 10^{-23}$ J/k.

$T = 273 + °C$.

$q = 1.6022 \times 10^{-19}$ C

Problem:

The forward vge drop of a power diode is $V_D = 1.2V$ at $I_D = 300A$. Assuming $n = 2$ and $V_T = 25.8$ mV, Find sat cunt I_S.

$$I_D = I_S \left(e^{V_D/nV_T} - 1\right) ; \quad 300 = I_S \left(e^{1.2/2 \times 25.8 \times 10^{-3}} - 1\right)$$

$\therefore I_S = 2.38371 \times 10^{-8}$ A.

BIPOLAR JUNCTION TRANSISTOR :- (BJT)

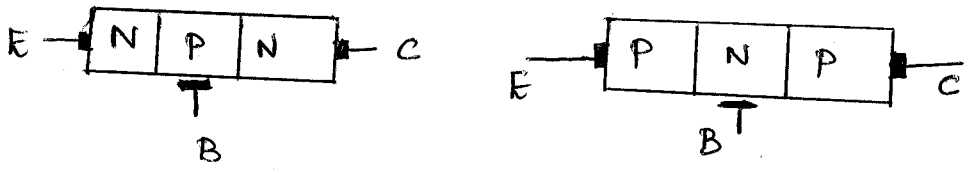
* A BJT is a three terminal device, whose output voltage, current, power are controlled by its input current. [current controlled device]

* It is a bipolar device. It is also called as power transistors in general. Amplification is the important property of the BJT.

* The BJT's are of two types

a) NPN b) PNP

E = emitter
B = Base
C = collector.



Construction :-

BJT has 3 regions namely emitter, base and collector.

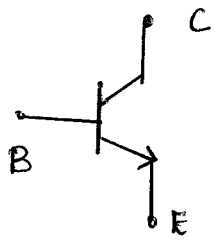
Emitter :-
It is a heavily doped region which supplies charge carriers [electrons or holes] to the other two regions.

Base :- It is the middle region that forms two PN Junctions. The base is thin compared to emitter and is a lightly doped region.

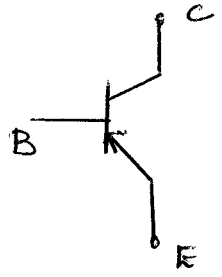
Collector :
It is a medium doped region which collects charge carriers

BJT has two junctions namely
a) Emitter-base junction (EB) b) collector-base junction (CB)

Symbols of BJT



NPN BJT



PNP BJT

Biasing of BJT (or) Modes of operation of BJT:-

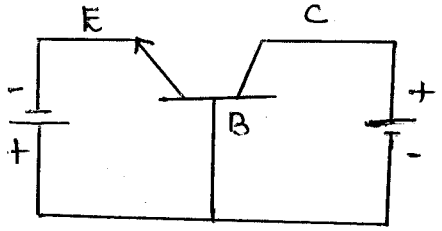
BIASING:-

Application of suitable dc voltages across the transistor terminals is called biasing.

There are three modes of operation (biasing) of BJT

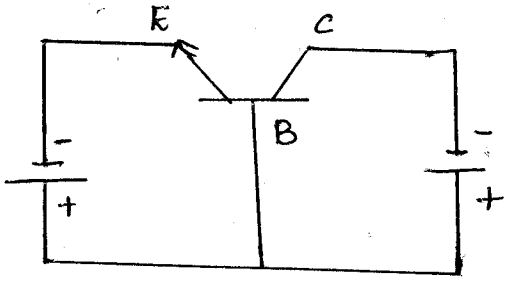
(i) Forward active mode:-

In this mode the emitter-base junction is forward biased and collector-base junction is reverse biased.



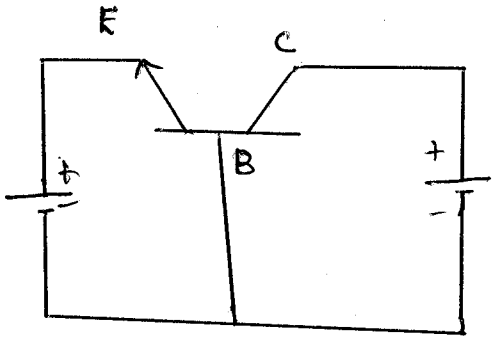
(ii) Saturation mode:-

Both the emitter-base and the collector-base junctions are forward biased.



(iii) Cut-off mode:-

Both the emitter-base and collector-base junctions are reverse biased.



Operation of BJT:-

FOR NPN:- (Operation due to movements of e^{-s})

* Emitter base is forward biased and collector base is reverse biased.

* The forward bias on the emitter causes the free e^{-s} in the N type emitter to flow towards the base region. This constitutes the emitter current (I_E)

* The free e^{-s} combine with holes in the base to constitute the base current (I_B)

* All e^{-s} do not get sufficient holes to combine in the base region and so travel towards the collector constituting the collector current [I_C].

* Here the current direction is opposite to flow of e^{-s}

FOR PNP:- (Operation due to movement of holes)

* Emitter base is forward biased and collector base is reverse biased.

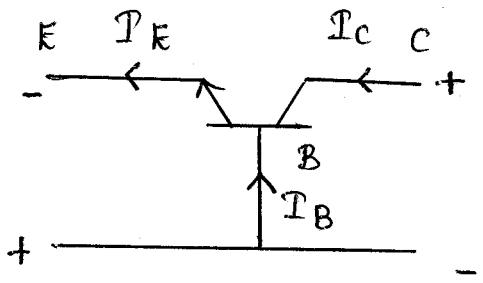
* Forward bias on emitter causes the holes in emitter to flow towards base region and constitute emitter cuut (I_E).

* Holes from emitter combines with e^{-s} in base to constitute base current [I_B]

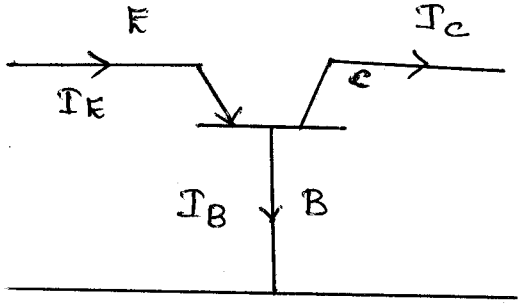
* All holes do not get sufficient e^{-s} to combine with in the base region and so they move towards collector and constitute the collector cuut [I_C].

* Current direction is same as that of the movement of holes.

NPN



PNP



$$I_E = I_B + I_C$$

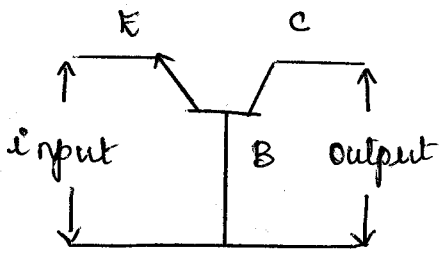
$$I_E \simeq I_C \qquad \because I_B \text{ is small}$$

BJT CIRCUIT CONFIGURATIONS:

* Depending on the terminals which are used as common terminals, the transistors can be connected in three different configurations.

1. Common base configuration:- (CB)

* Base is taken as common terminal.
* Input is applied between emitter and base.
* Output is taken between collector and base.



Common base current gain $= \alpha = \dfrac{I_C}{I_E}$

d.c current gain $= \alpha = \dfrac{I_C}{I_E}$

$$\alpha = \frac{I_C}{I_E} \; ; \quad \boxed{I_C = \alpha I_E}$$

α varies b/w 0.95 to 0.998.

$$I_E = I_B + I_C$$

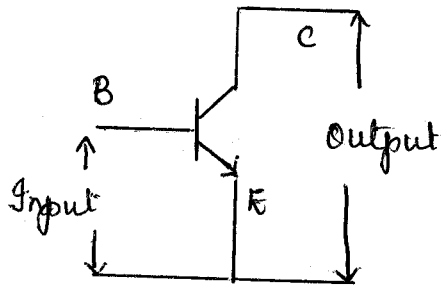
$$I_E = I_B + \alpha I_E$$

$$I_B = I_E - \alpha I_E = I_E (1-\alpha)$$

$$\therefore \boxed{I_B = I_E (1-\alpha)}$$

2. Common-emitter configuration:- (CE)

* Emitter is taken as common terminal.
* Input is applied between base and emitter.
* Output is taken between collector and emitter.



Common emitter current gain $= \beta = \frac{I_C}{I_B}$

Relationship between α and β:

we know that $I_E = I_B + I_C$

On dividing by I_E on both sides

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_E} \cdot 1$$

$$\therefore \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\alpha = \frac{I_C}{I_E} \; ; \; \beta = \frac{I_C}{I_B} \; ; \; \therefore \frac{I_E}{I_C} = \frac{1}{\alpha} \; ; \; \frac{I_B}{I_C} = \frac{1}{\beta}$$

On substituting for α and β

$$\therefore \frac{1}{\alpha} = \frac{1}{\beta} + 1 \Rightarrow \frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\therefore \boxed{\alpha = \frac{\beta}{1+\beta}}$$

The equation $\alpha = \frac{\beta}{1+\beta}$ can be written as

$$\alpha(1+\beta) = \beta$$

$$\alpha + \alpha\beta = \beta$$

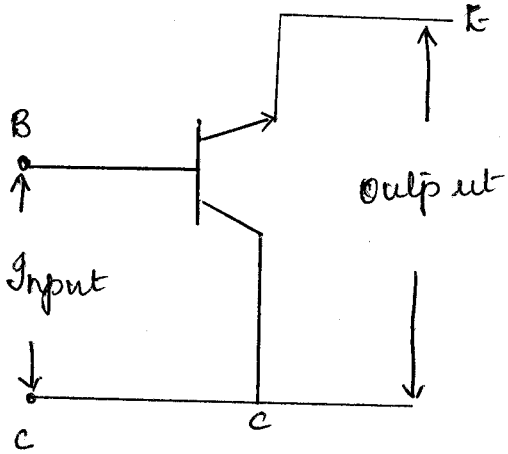
$$\alpha = \beta - \alpha\beta$$

$$\alpha = \beta(1-\alpha)$$

(or) $$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

3. common collector configuration :- (CC)

* collector is taken as common terminal.
* Input is given between base and collector.
* Output is taken between emitter and collector.



Common collector current gain $= \frac{I_E}{I_B} = \frac{I_E}{I_B} * \frac{I_C}{I_C}$ (on x lying and ÷ by I_C)

$$\Rightarrow \frac{I_E}{I_C} * \frac{I_C}{I_B} = \frac{1}{\alpha} * \beta$$

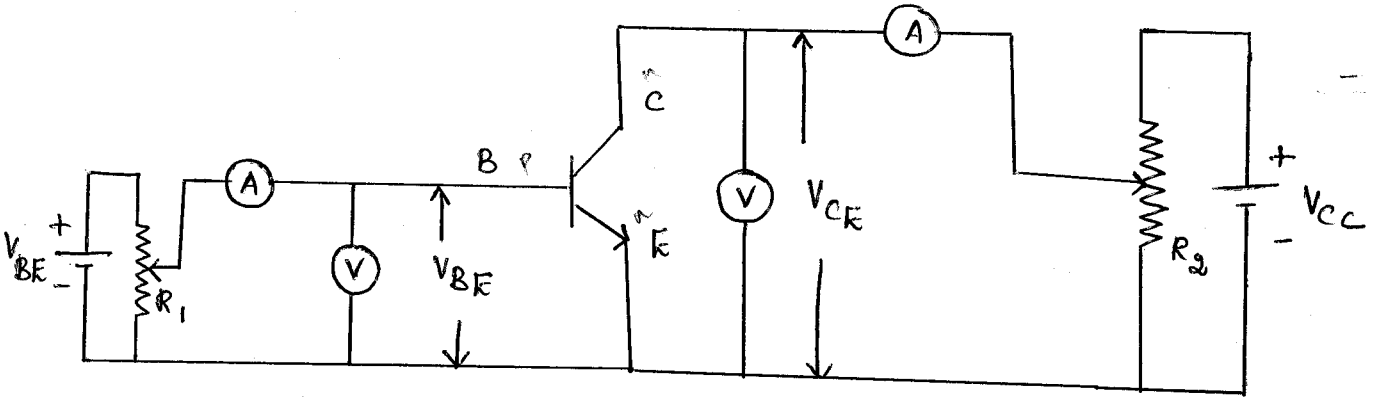
Substitute $\alpha = \frac{\beta}{1+\beta}$

$$\frac{1+\beta}{\beta} * \beta = 1+\beta$$

$\therefore$ Common collector current gain $= \frac{1}{\frac{\beta}{1+\beta}} * \beta$

V-I characteristics of BJT :

* The output chs of BJT is called as VI characteristics.



* The base current is adjusted to some constant value

* Then the collector to emitter voltage in increased in steps and the corresponding values of collector current is noted down.

* V-I characteristics is drawn by taking V_{CE} along x-axis and I_C along Y-axis.

* V-I chs can be drawn at any value of base current $[I_B = 0, 20, 40, 60\ \mu A \ldots]$

Output characteristics is divided into 3 regions.

a) Saturation region

b) Active region

c) Cut off region.

* when V_{CE} is increased above zero, the collector current increases to a saturation value.

* Saturation value depends on base current.

* When V_{CE} is further increased, the collector current I_C increases slightly.

* When base current is zero, a small collector current exists. However for practical purpose I_C is zero.

Cut off region:-

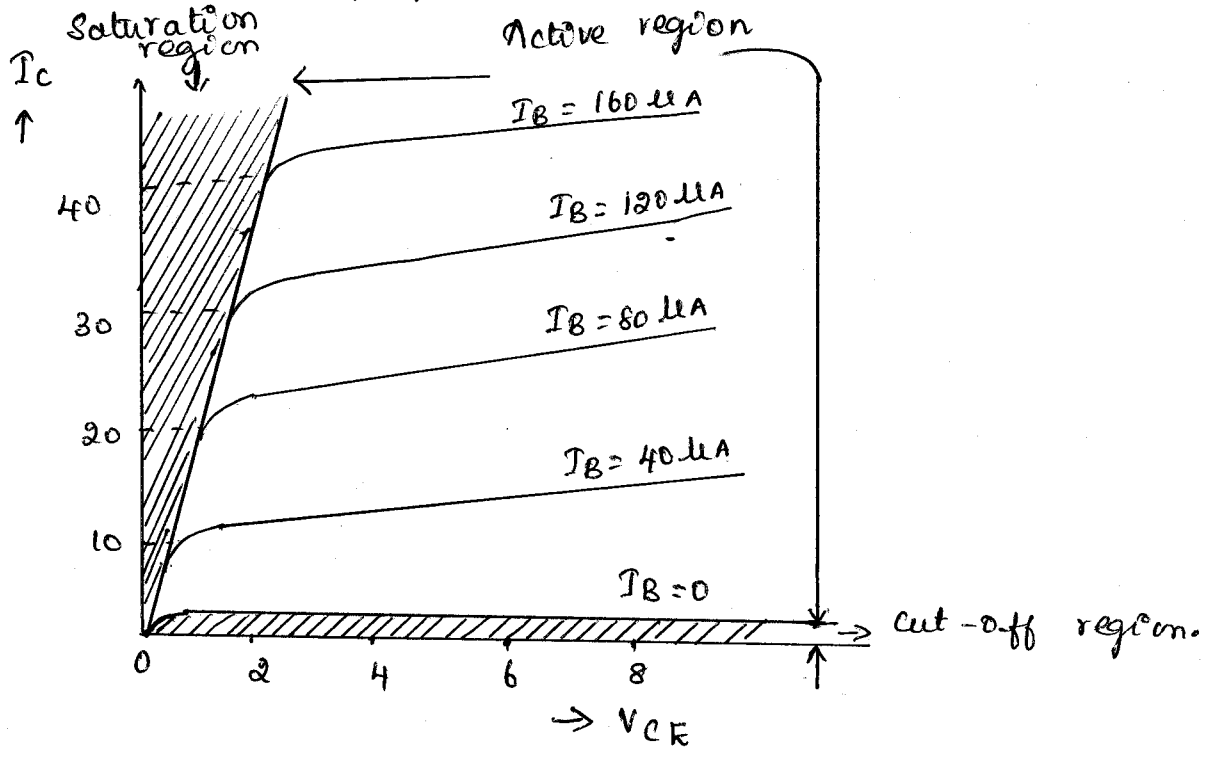
It is the region in the VI chs in which the transistor does not conduct (or) $I_C = 0$

Saturation region:-

It is the region in which the transistor conducts to the maximum extent decided by external components and supply voltage. I_C is maximum & V_{CE} is minimum.

Active region:-

It is the region in which the transistor collector current is proportional to the input base current.



Advantages of BJT:

* They have small turn ON and turn off times, ∴ their switching frequencies are higher.
* It has small turn - On losses.
* Base drive has full control over the operation of BJT.
* It does not require commutation circuits.
* It is a bipolar device.

Disadvantages of BJT:

* Drive circuit of BJT is complex.
* storage charge in base reduces switching frequencies.
* Negative temperature coefficient creates problems in paralleling of BJTs.

Applications of BJT:

* Switched mode power supplies.
* Bridge inverters.
* DC to DC converters.
* power factor correction techniques.

Problem 1:-

The common-base dc gain of a BJT is 0.967. If the emitter current is 10mA. what is the value of base current?

Given data; $\alpha = 0.967$

$I_E = 10mA$

$I_B = ?$

$I_E = I_B + I_C$

$\therefore I_B = I_E - I_C$.

$\alpha = \frac{I_C}{I_E}$; $\therefore I_C = \alpha I_E = 10 \times 10^{-3} \times 0.967 = 9.67 mA$.

$\therefore I_B = I_E - I_C = 10 - 9.67 = \boxed{0.33 mA}$

Problem 2:-

A BJT has $\beta = 150$. Calculate I_C and I_B if $I_E = 10mA$.

Given data:-

$\beta = 150$

$I_E = 10 mA$

$I_E = I_C + I_B$

$\alpha = \frac{I_C}{I_E}$; $\therefore I_C = \alpha I_E$

$\alpha = \frac{\beta}{1+\beta} = \frac{150}{1+150} = 0.9933$

$\therefore I_C = \alpha I_E = 0.9933 \times 10 mA = \boxed{9.933 mA}$

$\therefore I_B = I_E - I_C = 10 - 9.933 = 0.07 mA$

$\therefore \boxed{I_B = 0.07 mA}$

POWER MOSFET:-

* Metal Oxide semiconductor field effect transistor.
* It has 3 terminals : Gate, Source, Drain.
* The gate is insulated from the channel by means of a layer of SiO_2.
* ∴ MOSFET is also called as IGFET [Insulated Gate FET].
* Its a majority charge carrier, Unipolar device.
* It is a voltage controlled device. The Gate terminal has complete control over the operation of MOSFET.

MOSFET operates on two modes:

(i) Depletion mode :- Here a negative gate voltage is applied to decrease the width of the channel.

(ii) Enhancement mode :- Here a positive gate voltage is applied to increase the width of the channel.

There are two types of MOSFETs:-

a) Depletion type MOSFET.
b) Enhancement type MOSFET.

They differ in their construction. Both types have N-channel and P-channel MOSFETs.

a) DEPLETION TYPE MOSFET:-

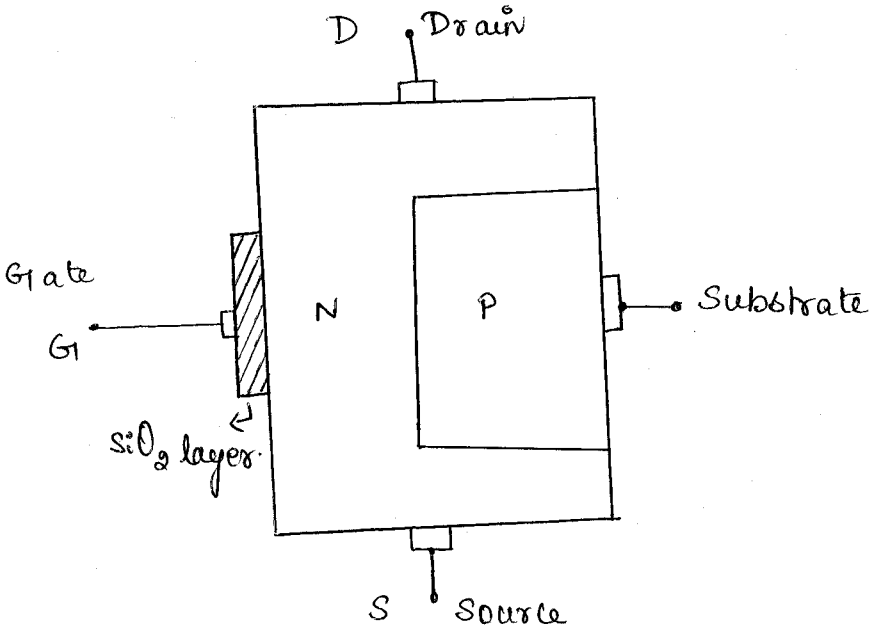
Construction:- (N-channel)

* It has an N type material.

* An insulated gate is placed on the left of the N-type material. (Gate is insulated by a layer of SiO_2)

* P-type material is on right of N-channel.

* Free e^{-s} flow from source to drain through N-channel.



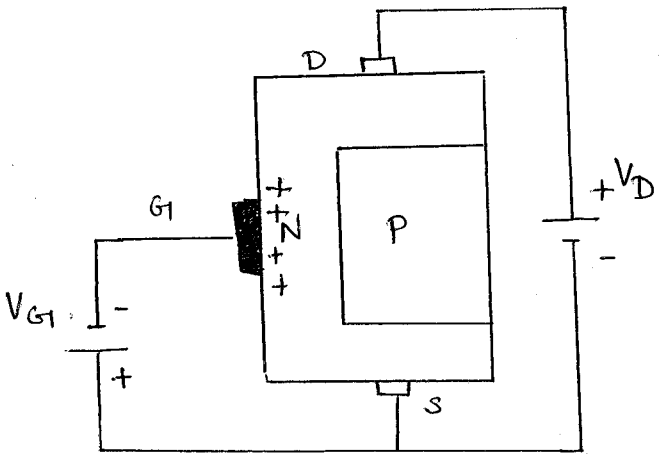
N-channel depletion type MOSFET

Depletion type MOSFET can operate on a) Depletion mode and b) Enhancement mode. ∴ Depletion type MOSFETs are also called as (DE) Depletion-enhancement MOSFET.

The operation of MOSFET can be explained by visualising the entire structure of MOSFET as a parallel plate capacitor. One plate is formed by gate, the other by the channel. The SiO_2 layer acts as a dielectric.

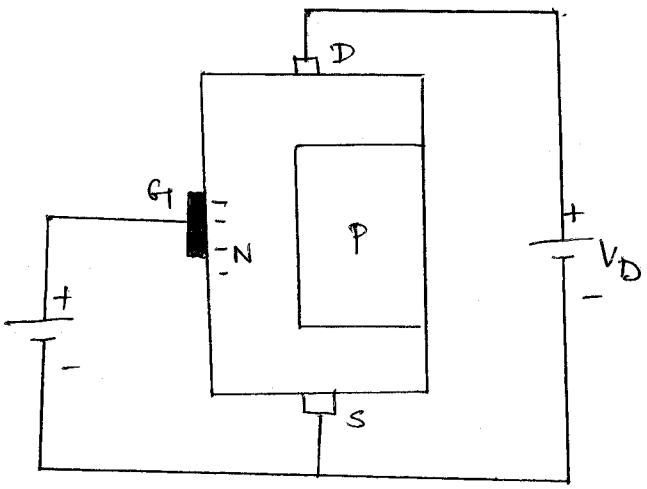
If one plate of capacitor is made negative, it induces a positive charge on the opposite plate.

Operation in DEPLETION MODE: (Gate vge should be negative)



* A Negative Gate Voltage should be applied (ie V_{G1} is -ve)
* -ve vge induces a +ve charge in the channel.
* So the electrons are repelled away. [Formation of depletion layer]
* As the -ve gate to source voltage is increased the N channel is depleted off of all the free e^{-s}. So the drain current is zero.
* This value of gate to source voltage at which the channel is depleted off of all the e^{-s}, [or] when the drain current is zero is called as $V_{GS(OFF)}$.

Operation in ENHANCEMENT MODE:



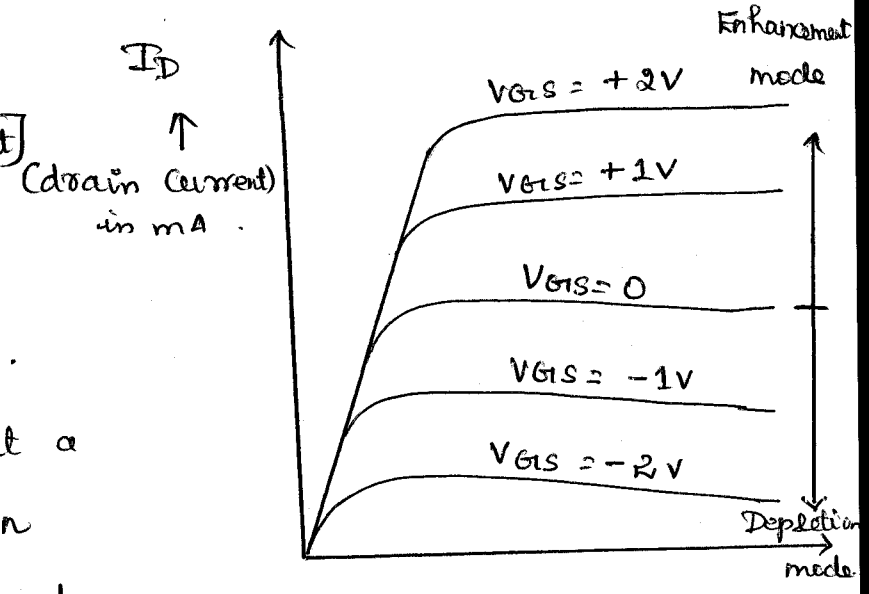
* To operate in this mode, the gate voltage must be positive.
* +ve voltage on the gate induces a -ve charge of the channel.
* This increases the no of free e^{-s} in the N channel.
* As the gate to source voltage is increased the no of free e^{-s} are further increased.
* This enhances the conduction of the channel.

V-I characteristics [or] Drain characteristics [or] O/P characteristics.

DEPLETION TYPE:

[Plotted b/w I_D Vs V_{DS}; V_{GS} = constant]

* For depletion mode the conduction will be only for -ve gate-source voltge (V_{GS}).
* V_{GS} should be maintained at a constant -ve value and then V_{DS} should be ↑ed in steps and corresponding values of I_D should be noted.
* different drain chs can be obtained for different values of V_{GS} (for eg $V_{GS} = -1, -2 \ldots\ldots$)

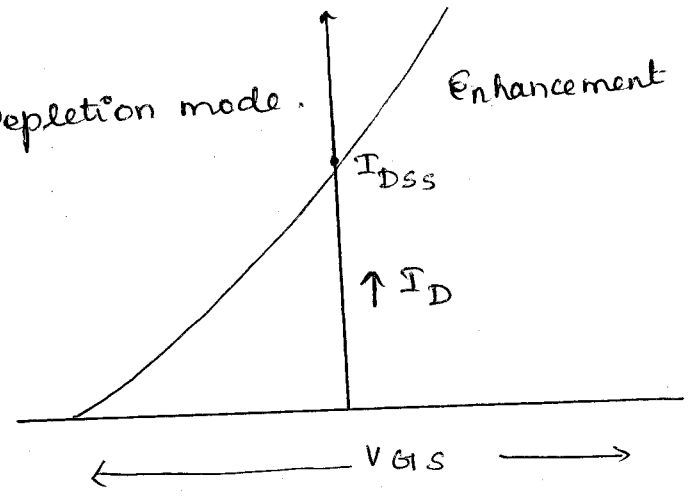


* For enhancement mode V_{GS} should be set to +ve voltages.
* V_{GS} is kept at constant +ve value, then V_{DS} is increased in steps and corresponding values of I_D is noted down.

Then a graph is plotted b/w I_D and V_{DS} keeping V_{GS} constant

Transfer characteristics: (or) Transconductance curves:

It is plotted b/w I_D and V_{GS} keeping V_{DS} constant.

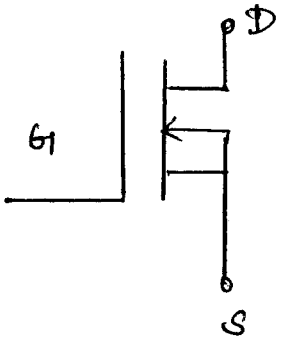


* Initially V_{GS} is = 0.
* V_{DS} is adjusted to bring the drain current (I_D) to a value I_{DSS}.
* Now the gate to source voltage is varied. ($V_{GS} = -1, -2$ for depletion mode
$V_{GS} = +1, +2$ for enhancement mode)

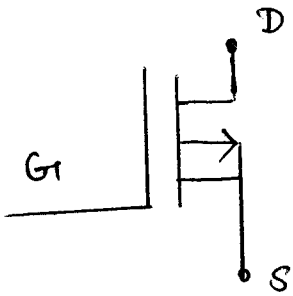
* **Depletion mode:-**
  * In this mode the V_{GS} is increased on the -ve side (ie $-1, -2 \cdots$).
  * With ↑ in V_{GS} the width of depletion layer increases and so the drain current reduces to zero.

* **Enhancement mode:-**
  * In this mode V_{GS} is ↑ed in the +ve side.
  * With ↑ in V_{GS} the no of free e^{s} in the channel increases and so the drain current I_D ↑es from the value I_{DSS}.

Symbol for Depletion type MOSFET:-



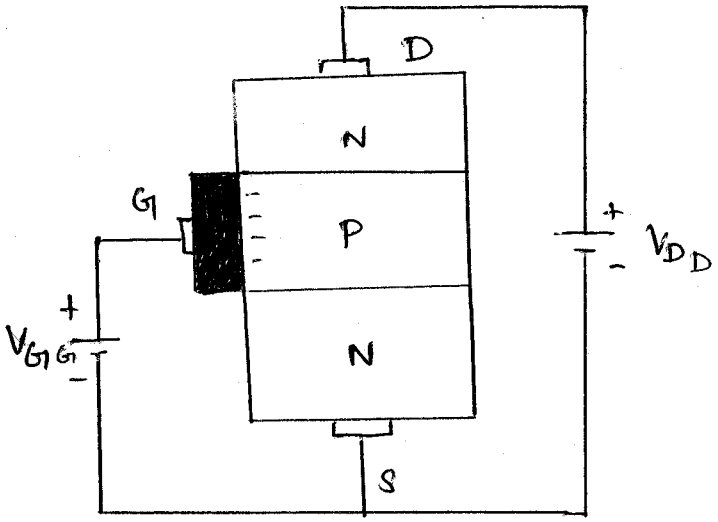
N - channel.



P- channel.

b) ENHANCEMENT TYPE MOSFET:

construction:-

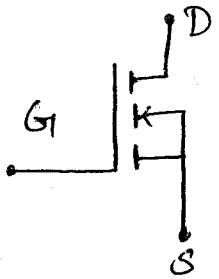


* It has no physical channel.
* SiO_2 layer is on whole of the P substrate.
* Gate voltage is always +ve.
* when $V_{GS} = 0$; V_{DD} forces the e^{-s} from source to drain. But, the p region does not allow the e^{-s} through it $\therefore$ $I_D = 0$ at $V_{GS} = 0$.
* Now if some +ve values of V_{GS} is applied, it induces a -ve charge in the P region. This is formed by attracting e^{-s} from the source.
* As V_{GS} is further increased, it attracts more e^{-s} from the source. This forms a thin layer of e^{-s} in the P-material. [This layer of free e^{-s} is called N-type inversion layer].
* This is similar to forming an N channel in a P materials.

So now there is flow of e^{-s} from source to drain.

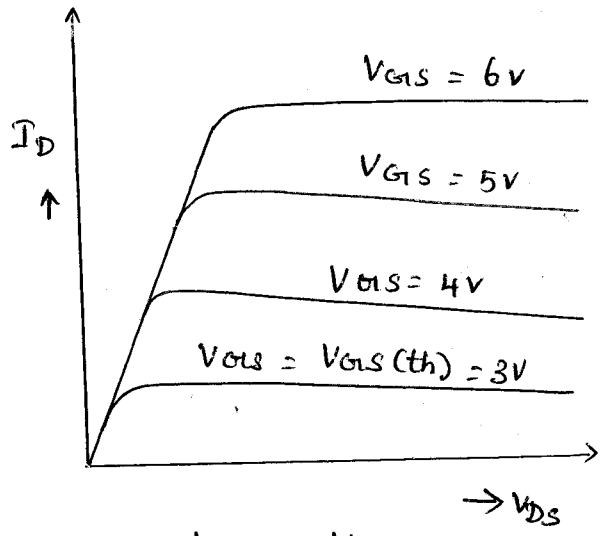
* This value of V_{GS} at which the drain current starts flowing [or] the inversion layer is produces is called as the $V_{GS(th)}$ (Threshold voltage) (or) V_{GST}.

Symbol:-



V-I characteristics [or] Drain characteristics:-

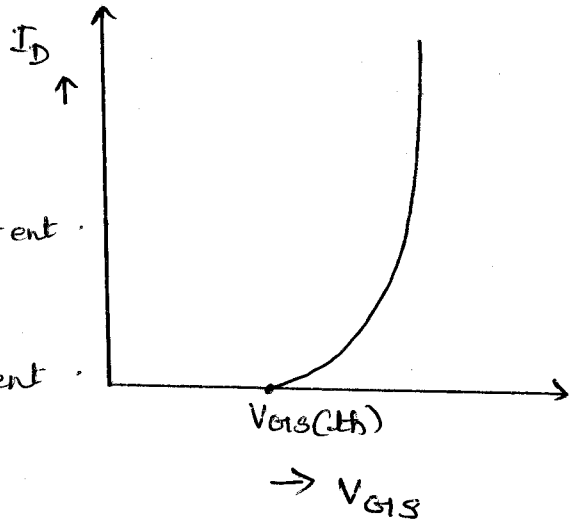
* different V-I chs are drawn for different values of V_{GS}.
* Drain current will be zero for $V_{GS} < V_{GS(th)}$.
* The first V-I chs is drawn for $V_{GS} = V_{GS(th)}$.



* V_{GS} is maintained constant at some +ve values, then V_{DS} is ↑ed in steps and the corresponding values of I_D is noted down.
* Graph is plotted b/w I_D and V_{DS}.

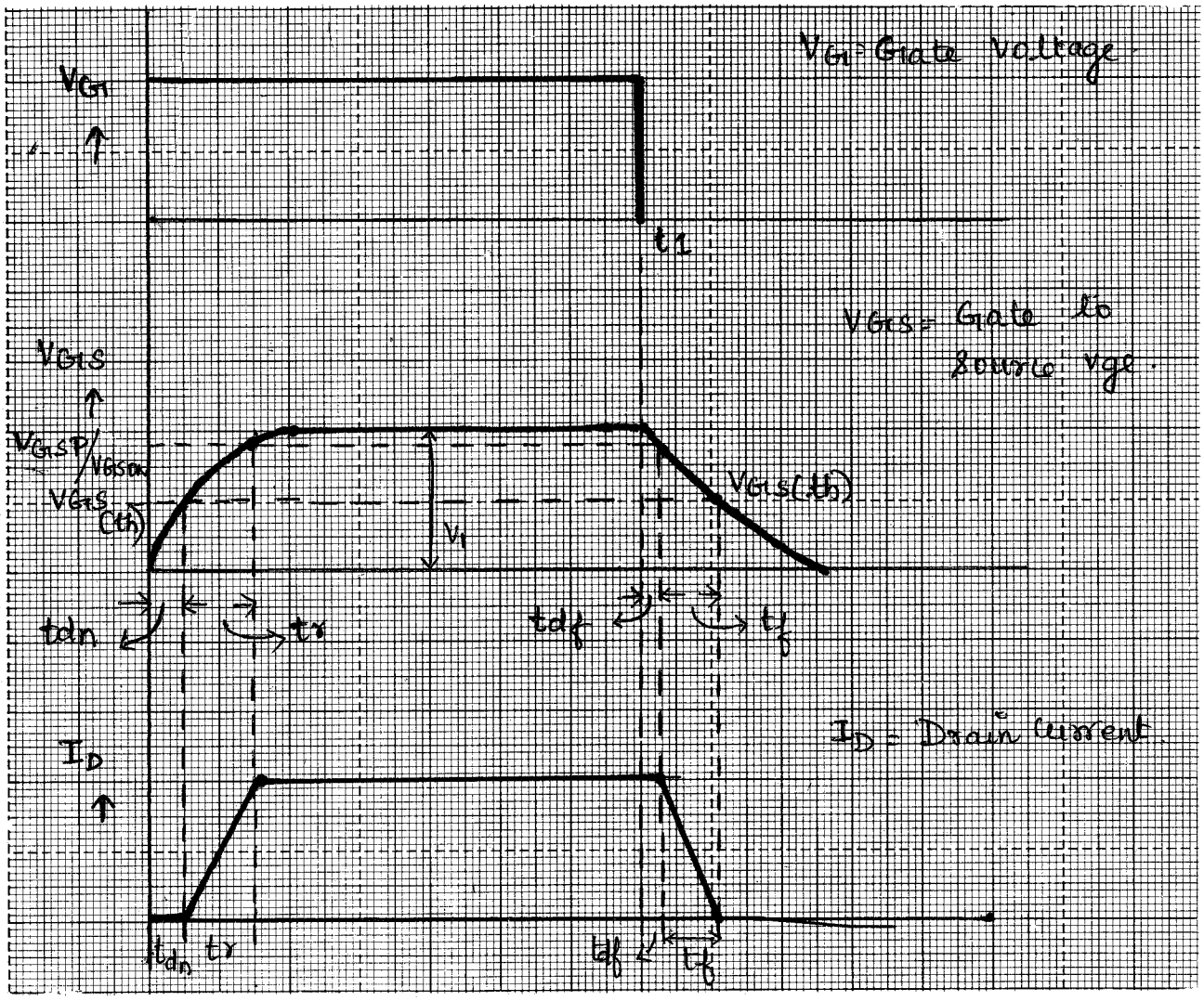
Transfer characteristics:-

* V_{DS} is increased and maintained at a constant value.
* Now V_{GS} is varied.
* Till $V_{GS} = V_{GS(th)}$ the drain current $I_D = 0$.
* After $V_{GS} > V_{GS(th)}$ the drain current increases.



Switching characteristics:- (Turn ON / OFF characteristics):-

The switching characteristics of the MOSFET is influenced to a large extent by the internal capacitance of the device and the internal impedance of the gate drive circuit.



* when the gate voltage (V_G) is applied, the gate to source vge (V_{GS}) does not increase immediately. There is a initial delay during which the input capacitance charges.

* The initial time delay is t_{dn} (turn on time delay):-

It is the time taken for the gate to source voltage (V_{GS}) to increase to threshold value. ($V_{GS(th)}$ or V_{GST}) Till the vge $V_{GS} = V_{GS(th)}$ the drain current is zero.

* At the end of t_{dn} the drain cuut I_D ↑es.

* The next time delay is rise time (t_r):-

It is the time taken for the drain current to increase from zero to the maximum value. [OR] It is the

time taken by the V_{GS} to rise from $V_{GS(th)}$ to V_{GSP} or $V_{GS(on)}$. At this voltage the device is completely in its ON state.

[t_{ON} can be reduced by using low impedance gate drive source]

$\therefore$ Turn on time $\boxed{t_{on} = t_{dn} + t_r}$

* The turn off process starts soon after the gate voltage is removed at time t_1.
* There is a time delay during which the input capacitance discharges.
* There is a turn off time delay (t_{df}) during which the gate to source voltage reduces from V_1 to V_{GSP}.
* Then we have a time delay called as t_f (fall time) during which the gate to source V_{gs} reduces from V_{GSP} to $V_{GS(th)}$
* As the voltage reaches $V_{GS(th)}$ the drain current reaches Zero.
* At $V_{GS} < V_{GS(th)}$ the MOSFET is completely OFF.

$\therefore$ Turn off time $\boxed{t_{off} = t_{df} + t_f}$

Merits of MOSFET:-

* Short turn ON and turn OFF time $\therefore$ the switching frequency is high. They operate at high frequency.
* Do not require commutation circuit.
* Gate has full control over the operation of MOSFET.
* Simple drive circuits.
* +ve temperature coefficient of resistance. so paralleling of MOSFET is easy.

Demerits of MOSFET:

* On state loss is high.
* Used for low power applications.
* Static charge problems.

Applications:

* High frequency and low power inverters.
* High frequency SMPS
* High frequency inverters and choppers.
* Low power ac and dc drives.

Difference between BJT and MOSFET:

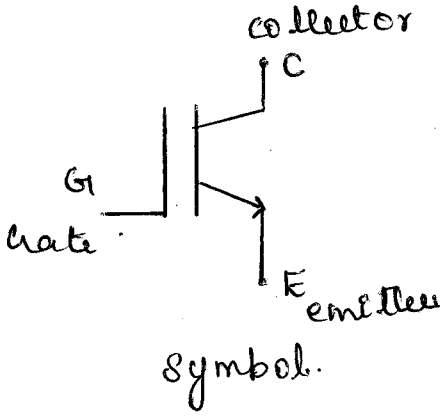
BJT	MOSFET
1. It is a bipolar device.	It is a unipolar device.
2. It is controlled by base.	It is controlled by gate.
3. It is a current controlled device.	It is a Vge controlled device.
4. -ve tempt coeff of Resistance.	+ve tempt coeff of resistance.
5. Paralleling of BJT is difficult.	Paralleling of MOSFET is simple.
6. ON state loss is low.	ON state loss is high.
7. Switching loss is high.	switching loss is less.
8. Drive circuit is complex.	Drive circuit is simple.
9. Switching frequency is less.	Switching frequency is high.
10. Used in high power applications.	Used in low power applications.
11. High voltage and current rating.	Less voltage and curnt rating.

IGBT:- Insulated Gate Bipolar Transistor:

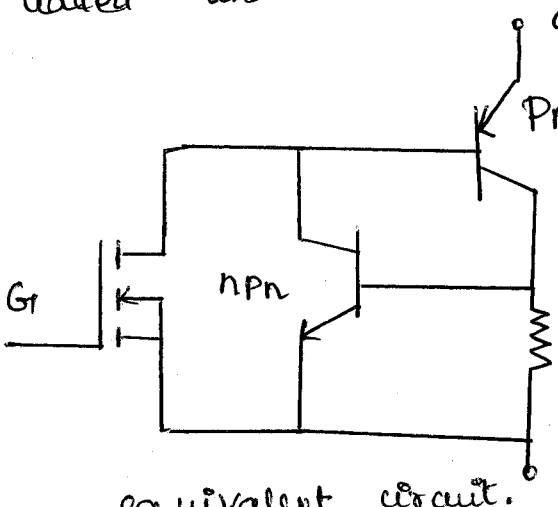
* IGBT is obtained by combining the properties of BJT and MOSFET.
* The gate circuit of MOSFET and collector - emitter circuit of BJT is combined together to form the IGBT.
* IGBT has high input impedance like MOSFET and low ON state conduction loss like BJT, but there is no secondary breakdown problem like BJT.

Construction:- It is a voltage controlled device. It is bipolar

* It is made of four alternate PNPN layers.
* On p^+ substrate a high resistivity "n" layer is grown epitaxially.
* The thickness of "n" layer determines the voltage blocking capability of the device.
* On the other side of p^+ substrate a metal layer is deposited to form the collector terminal.
* Now P-regions are diffused in the epitaxially grown 'n' layer, and then n^+ regions are diffused in P-regions.
* The SiO_2 layer is added and the emitter and gate terminal are formed.

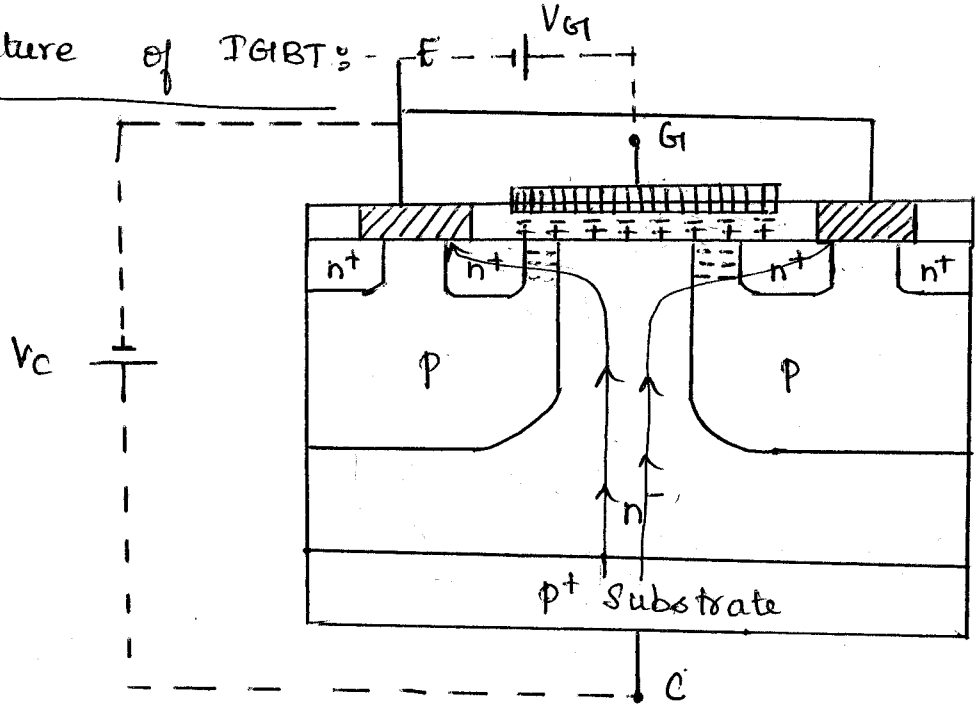


Symbol.



equivalent circuit.

Structure of IGBT:-



Working :-

* When Gate is +ve with respect to emitter and when V_{GE} is $> V_{threshold}$, an n-channel is formed in the P-regions as in a MOSFET. This shorts the n^- region with n^+ region.

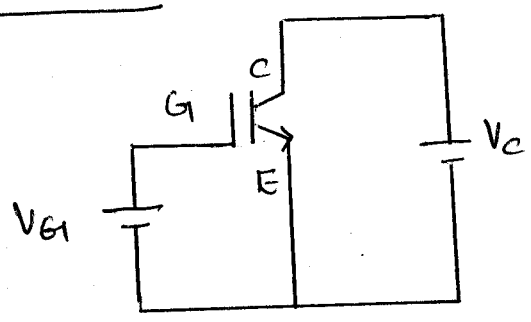
* An electron movement in the n-channel causes substantial hole injection from P+ substrate layer into the epitaxial n^- layer. ∴ a forward current flows.

Equivalent circuit:-

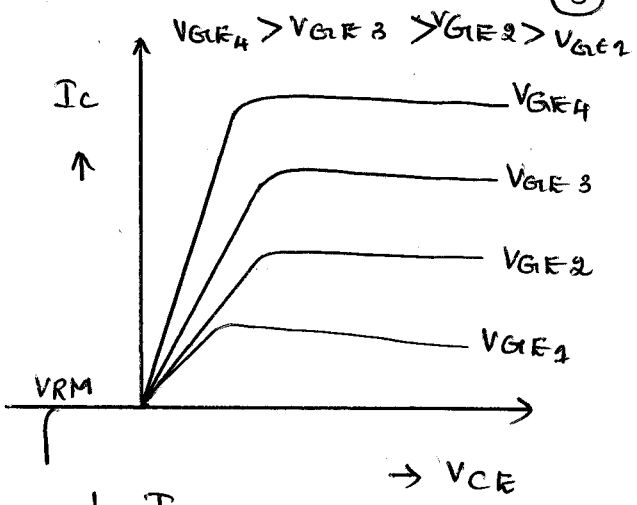
* The three layers P^+, n^-, P contributes an pnp transistor with P^+ as emitter, n as base and P as collector.

* n^-, P, n^+ serves as npn transistor; here n^- acts as collector.

V-I characteristics:-

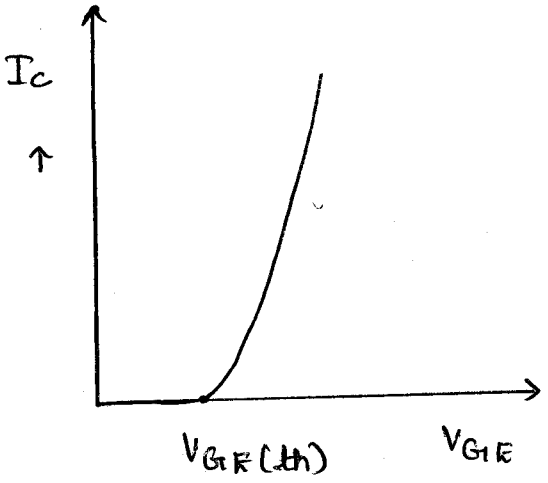


* V-I chs are drawn for different values of V_{GE}.
* when V_{GE} is > V_{GE} (threshold) IGBT turns ON.
* By keeping V_{GE} constant, the value of V_{CE} is varied and corresponding values of I_C is noted down.
* A graph is plotted between V_{CE} and I_C.



Transfer characteristics:-

* V_{CE} is increased and maintained at a constant value.
* Now V_{GE} is varied in steps and I_C is noted down.
* Till $V_{GE} = V_{GE(th)}$ the collector current is zero.
* After V_{GE} is > $V_{GE(th)}$ the collector current increases.



Switching characteristics:-

TURN ON:-

* V_{GE} is normally negative. V_{GE} is made positive to turn ON IGBT.
* As gate vge is ↑ed, V_{GE} ↑. when $V_{GE} = V_{GE(th)}$ the collector current I_C starts to flow.
* Time taken for V_{GE} to rise and reach $V_{GE(th)}$ (or) the time for I_C to start ↑ing is called as turn on delay time t_{dn}.

* After $V_{GE(th)}$, the collector current I_c starts rising. The time for I_c to rise and reach its max value is called as rise time for current (t_{ri}).

* When I_c reaches its max value, IGBT is in its ON state. When a device is in its ON state it is said to be short circuited and so the voltage across it is equal to zero.

* ∴ when IGBT is on the V_{CE} vge starts reducing to a value nearly equal to zero. Here it falls to a value V_{CES} (Saturated value). (or) $V_{CE(ON)}$

* This time taken for voltage V_{CE} to fall and reach its saturated value V_{CES} is called as fall time for voltage (t_{fv})

∴ the turn ON time $\boxed{t_{ON} = t_{dn} + t_{ri} + t_{fv}}$

These time delays are due to two reasons.

→ Gate – collector capacitance will ↑ in MOSFET portion of IGBT at low VCE.

→ PNP transistor portion of IGBT travels (or) moves to the ON state more slowly than the MOSFET Portion of IGBT.

TURN OFF:

* IGBT is turned OFF by removing the gate voltage.

* when V_{GE} is reduced, V_{GEK} starts to fall and V_{CE} starts ↑ing. [gate V_{GE} ↓]

* Turn off delay time (t_{df}) is the time when V_{GEK} ↓ and V_{CE} ↑. V_{CE} ↑ at the end of t_{df}.

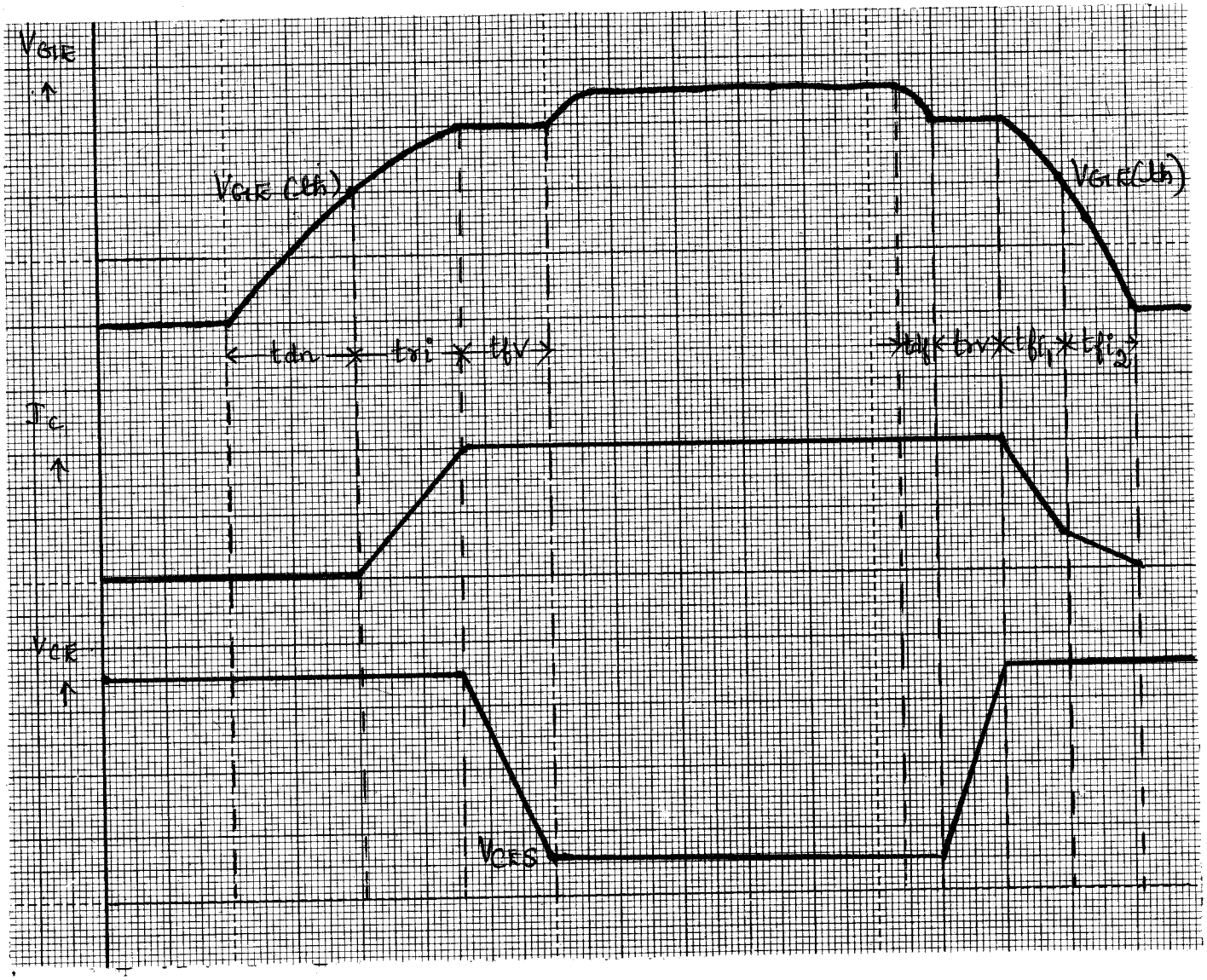
* V_{CE} ↑ and reaches its max value. The time taken for V_{CE} to rise and reach its full value is called as rise time for voltage (t_{rv}).

* As V_{GEK} ↓ and reaches $V_{GEK(th)}$ the drain current reduces to zero. Time interval t_{fi_1} is is the fall time for current. It is the turn off interval of the MOSFET section of IGBT.

* Here the current I_c is not zero but a small current flows due to the stored charge in n^- drift region. This is the internal BJT current.

* This tailing of current (due to BJT internal current) takes place during the interval t_{fi_2}. It is the turn off interval of the BJT section of IGBT.

∴ Turn off time $\boxed{T_{OFF} = t_{df} + t_{rv} + t_{fi_1} + t_{fi_2}.}$



Merits of IGBT:-

* Vge controlled device.
* less ON state loss.
* High switching freq
* No commutation circuit.
* Gate has full control over operation.
* flat tempt coefficient.

Demerits of IGBT:-

* Static charge problem.
* costlier than BJT and MOSFET.

Applications:

* AC motor drives.
* Dc to Dc power supplies
* UPS system.
* Harmonic compensators.

SCR: Silicon controlled Rectifier:

* A Thyristor is a four layer PNPN device. It has 3 junctions.

* Thyristors are used specifically for high power switching applications such as control of a.c power to load, motor speed control.

Types of thyristor:-

* Unidirectional thyristor:

The thyristors which conduct in forward direction only are known as unidirectional thyristors.

(eg) SCR - Silicon controlled rectifier.

LASCR - Light activated silicon controlled rectifier.

SCS - Silicon controlled switch.

* Bidirectional thyristor:-

The thyristors which can conduct in forward as well as in reverse direction are known as bidirectional thyristor.

(eg) TRIAC - Triode AC switch.

Triggering devices:-

The devices which generate a control signal to switch the device from non-conducting to conducting state is called as triggering device.

(eg) Diode AC switch - DIAC ; UJT : Uni Junction Transistor.

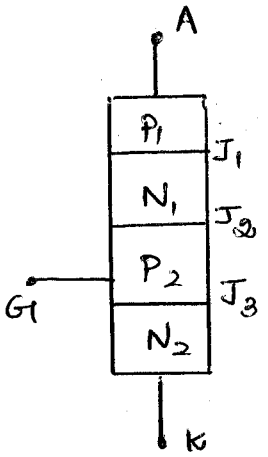
SUS - Silicon Unilateral switch.

SBS - Silicon Bilateral switch.

Silicon controlled Rectifier:-

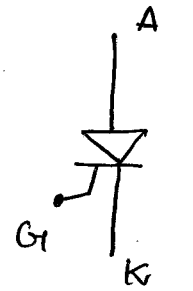
* SCR is a Unidirectional device.
* It is a current controlled device.
* It is a semi controlled device, because the gate terminal can be used to switch ON the SCR, and switching OFF cannot be done by the gate signal.

Construction:-



* SCR consists of four layers forming a Pnpn structure.
* It has 3 junctions - J_1, J_2, J_3.
* It has 3 terminals anode - A, cathode - K and gate - G_1.
* Anode is taken out from P_1 layer, cathode is taken out from N_2 layer. Gate is taken out from P_2 layer.

Symbol of SCR:



* SCR can be biased in two modes.
  - → Forward biased mode when the anode to cathode voltage is +ve.
  - → Reverse biased mode when the anode is -ve w.r.t. cathode.

SCR Operation:-

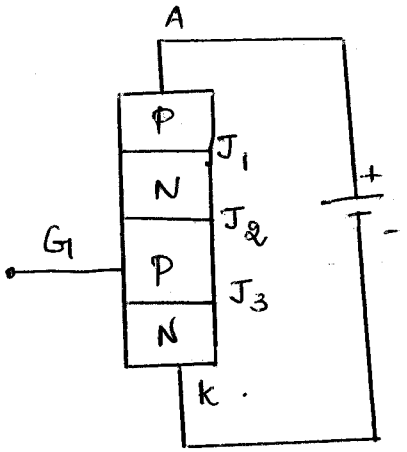
* Operation of SCR is explained by the help of four modes.

1. Forward blocking mode.
2. Forward conducting mode.
3. Reverse blocking mode.
4. Reverse conducting mode.

1. Forward blocking mode:-

(With gate open)

* A positive voltage is applied between anode (A) and cathode (K) of SCR.



* Anode is +ve w.r.t. Cathode.

* Junction J_1 and J_3 are forward biased and Junction J_2 is reverse biased.

* ∴ A depletion layer is formed in J_2. ∴ No current flows from anode to cathode.

* But a small leakage current flows due to the existence of leakage carriers in the junction J_2.

2. Forward conducting mode:-

* As the applied voltage is increased, the junction J_2 will undergo avalanche breakdown and loose its blocking ability.

* This voltage at which the junction breaks down is called as V_{BO} [Forward break over voltage, (or) Threshold voltage].

* SCR acts like a closed switch, and the current flowing from anode to cathode increases.

* At $V_{AK} > V_{BO}$, SCR turns ON.

* After SCR is ON, the voltage across the device reduces.

3. Reverse blocking mode:

* If anode is made -ve w.r.t. cathode, the junctions J_1 and J_3 are reverse biased and J_2 is forward biased.

* There is no flow of current, except for the leakage current through the device due to the leakage carriers.

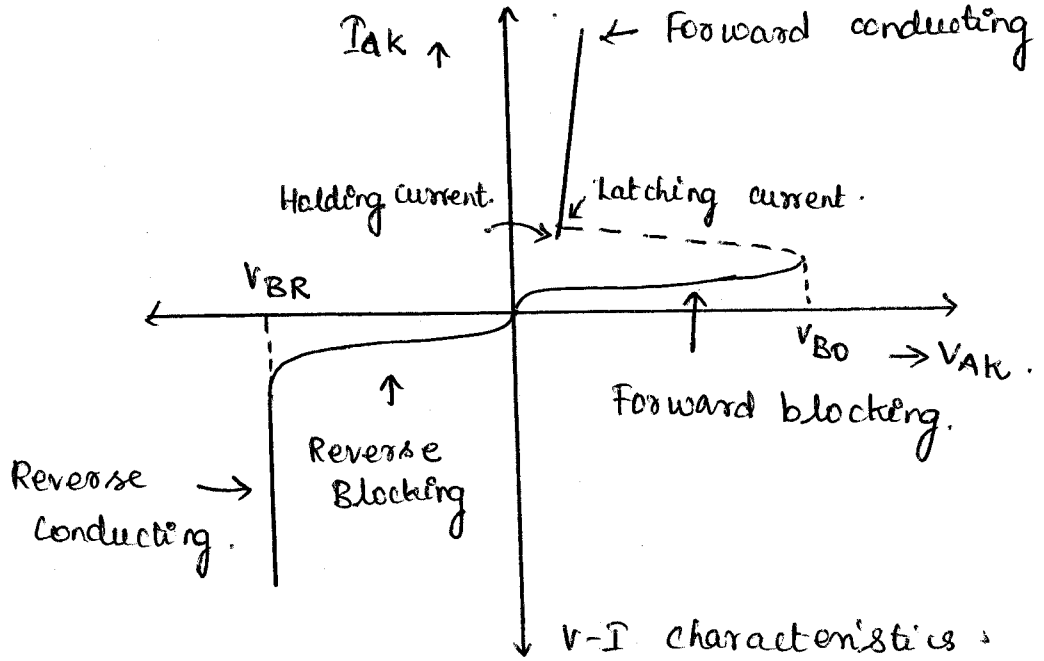
4. Reverse conducting mode:-

* As the reverse voltage is further increased, at the reverse breakdown voltage (V_{BR}) avalanche breakdown occurs at junction J_1 and J_3.

* SCR acts as a closed switch in reverse direction.

* A large current gives rise to more losses in SCR, dissipating in form of heat, thereby damaging the SCR.

* So the value of V_{AK} should not be increased beyond V_{BR} in the reversed biased condition.



Latching current (I_L) :-

It is the minimum anode current required to switch (latch) the SCR from OFF state to ON state.

Holding current (I_H) :-

It is the minimum anode current required to hold the SCR in ON state

(or)

It is the minimum current below which the device will move from ON state to OFF state.

Peak reverse voltage :-

It is the maximum voltage that can be applied across the SCR in reverse biased condition.

Peak inverse voltage :-

It is the maximum voltage which the device can safely withstand in its OFF state.

ON state voltage :-

The voltage which appears across the device during its ON state is known as its ON state vge.

Rate of rise of voltage $\frac{dV}{dt}$:-

The rate at which the voltage across the device rises without triggering the device is known as its rate of rise of voltage.

Current rating :-

The current carrying capacity of the device is known as its current rating.

Two transistor analogy of SCR:-

* Two transistor analogy of an SCR is obtained by splitting the two middle layers into two seperate parts.

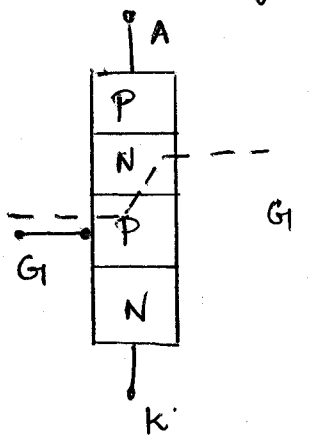


fig (A)

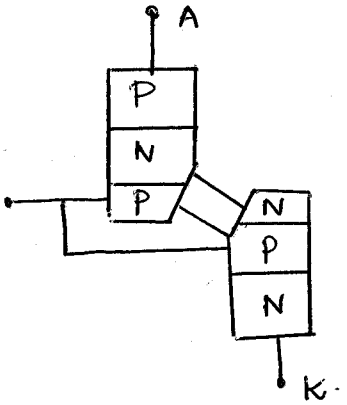


fig (B)

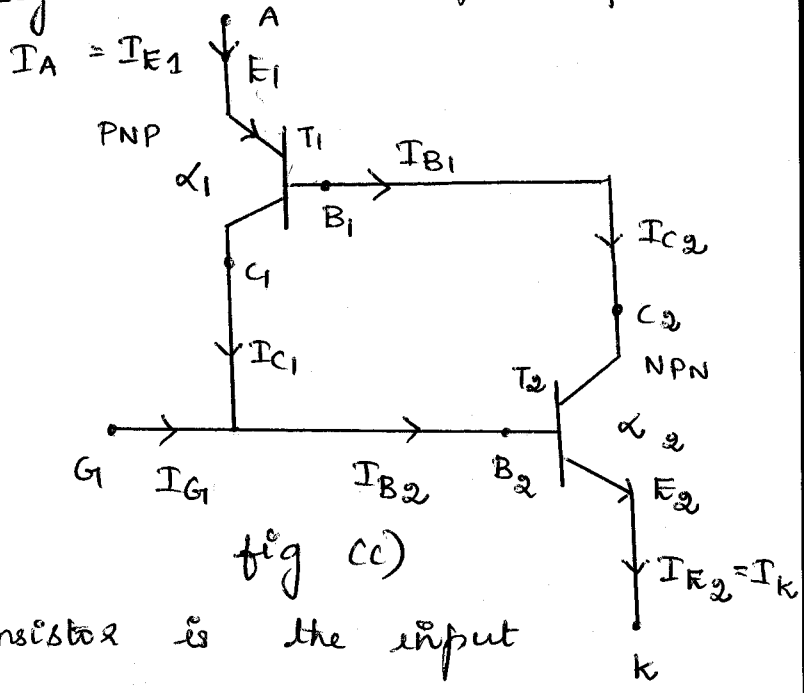


fig (C)

* O/p of PNP transistor is the input for NPN transistor.

* Even when the gate voltage is removed the transistor continue to conduct because they are connected back to back.

* without gate pulse, a large value of V_{AK} is required to turn ON SCR.

* With gate pulse a small voltage is enough to make the SCR conduct.

Current gain in forward direction $= \alpha = \frac{I_C}{I_E}$.

let α_1, α_2 be the current gain of transistor T_1 and T_2.

I_{CBO1}, I_{CBO2} be the leakage current in transistor T_1 and T_2.

From fig (C)

$$I_A = I_{E1} \; ; \; I_K = I_{E2} \; ; \; I_{B1} = I_{C2}$$

when $I_G = 0$; $I_{C1} = I_{B2}$.

$$\alpha_1 = \frac{I_{C1}}{I_{E1}} \quad ; \quad \alpha_2 = \frac{I_{C2}}{I_{E2}}.$$

$$\therefore I_{C1} = \alpha_1 I_{E1} \quad ; \quad \alpha_2 I_{E2} = I_{C2}$$

On including the values of leakage current.

$$I_{C1} = \alpha_1 I_{E1} + I_{CBO1}$$

$$I_{C2} = \alpha_2 I_{E2} + I_{CBO2}$$

$$I_A = I_{E1} = I_{B1} + I_{C1}$$

$$\therefore I_A = I_{B1} + I_{C1} \qquad \because I_{B1} = I_{C2}$$

$$\therefore I_A = I_{C2} + I_{C1}$$

$$I_A = \alpha_2 I_{E2} + I_{CBO2} + \alpha_1 I_{E1} + I_{CBO1}$$

$$\because I_{E2} = I_K \quad ; \quad I_{E1} = I_A$$

$$I_A = \alpha_2 I_K + \alpha_1 I_A + I_{CBO1} + I_{CBO2}$$

$$I_A - \alpha_1 I_A = \alpha_2 I_K + I_{CBO1} + I_{CBO2}$$

$$I_A (1 - \alpha_1) = \alpha_2 I_K + I_{CBO1} + I_{CBO2} \rightarrow (A)$$

$$\boxed{I_A = \frac{\alpha_2 I_K + I_{CBO1} + I_{CBO2}}{(1 - \alpha_1)}}$$

On neglecting the values of leakage current.

$$I_A = \frac{\alpha_2 I_K}{1 - \alpha_1} \quad (or)$$

$$\frac{I_A}{I_K} = \frac{\alpha_2}{1 - \alpha_1}$$

From eqn (A)

$$I_A(1-\alpha_1) = \alpha_2 I_K + I_{CBO1} + I_{CBO2}$$

with gate current

$$I_K = I_A + I_{G1}$$

$$\therefore I_A(1-\alpha_1) = \alpha_2 (I_A + I_{G1}) + I_{CBO1} + I_{CBO2}$$

$$I_A(1-\alpha_1) = \alpha_2 I_A + \alpha_2 I_{G1} + I_{CBO1} + I_{CBO2}$$

$$I_A(1-\alpha_1) - \alpha_2 I_A = \alpha_2 I_{G1} + I_{CBO1} + I_{CBO2}.$$

$$I_A(1-(\alpha_1+\alpha_2)) = \alpha_2 I_{G1} + I_{CBO1} + I_{CBO2}$$

$$\boxed{I_A = \frac{\alpha_2 I_{G1} + I_{CBO1} + I_{CBO2}}{1-(\alpha_1+\alpha_2)}} \rightarrow \text{eqn (B)}$$

On neglecting leakage cumt

$$I_A = \frac{\alpha_2 I_{G1}}{1-(\alpha_1+\alpha_2)}$$

$$\frac{I_A}{I_{G1}} = \frac{\alpha_2}{1-(\alpha_1+\alpha_2)}$$

From eqn B.

* when $\alpha_1+\alpha_2 = 0$; i.e., $\alpha_1 = 0$; $\alpha_2 = 0$ there is no conduction of SCR [current = 0].

* when $\alpha_1+\alpha_2 = 1$; $I_A \rightarrow \infty$ (large current). ∴ SCR will turn ON.

* The methods of turning ON SCR are in fact the methods of making $\alpha_1+\alpha_2$ to approach unity.

Methods of turning ON SCR:-

The various methods to turn ON an SCR are.

a) Forward voltage triggering.
b) Thermal (or) temperature triggering.
c) Radiation (or) Light triggering.
d) $\frac{dv}{dt}$ triggering.
e) Gate triggering.

a) Forward voltage triggering:

* In this mode a forward voltage is applied between anode and cathode.

* Junction J_1 and J_3 is forward biased and J_2 is reverse biased.

* No current flows due to depletion region in J_2. [except for leakage current].

* As V_{AK} is further increased, at a voltage V_{BO} (forward breakover voltage) the junction J_2 undergoes avalanche breakdown and so a current flows and the device tends to turn ON (even when gate is open).

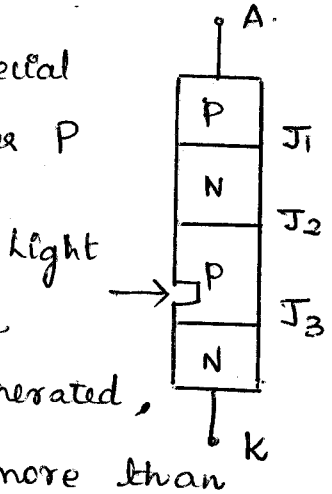
b) Thermal (or) temperature triggering:-

* The width of depletion layer of SCR decreases with increase in junction temperature.

* ∴ in SCR when V_{AK} is very near its breakdown vge, the device is triggered by ↑ing the junction tempt.

* By ↑ing the junction tempt the reverse biased junction collapses making the device conduct.

c) Radiation triggering (or) Light triggering :



* For light triggered SCRs a special terminal niche is made inside the inner P layer instead of gate terminal.

* When light is allowed to strike this terminal, free charge carriers are generated,

* When intensity of light becomes more than a normal value, SCR starts conducting.

* This type of SCRs are called as LASCRs.

d) $\frac{dv}{dt}$ triggering :-

* When the device is forward biased; J_1, J_3 are forward biased, J_2 is reverse biased.

* J_2 behaves as a capacitor, due to the charges existing across the junction.

* If voltage across the device is V, the charge by Q and capacitance by C then;

$$i_c = \frac{dQ}{dt} \qquad \because Q = CV$$

$$i_c = \frac{d(CV)}{dt} = C\cdot\frac{dv}{dt} + V\cdot\frac{dC}{dt} \qquad \frac{dC}{dt} = 0.$$

$$\therefore\ i_c = C\cdot\frac{dv}{dt}.$$

∴ If the rate of change of voltage across the device is large the device may turn ON even if the voltage across device is small

e) Gate triggering:-

* Applying a positive voltage between gate and cathode can turn ON a forward biased thyristor.

* When a +ve voltage is applied at the gate terminal, charge carriers are injected in the inner P-layer, thereby reducing the depletion layer thickness.

* As voltage ↑, carrier injection ↑, ∴ the V_{ge} at which forward break over occurs ↓.

Three types of signals are used for gate triggering.
(i) D.C signal. (ii) A.C signal (iii) Pulse signal.

1. D.C gate triggering:-

* A d.c voltage of proper polarity is applied between gate and cathode. (gate in +ve w.r.t. cathode).

* When applied voltage is sufficient to produce the required gate current, the device starts conducting.

* One drawback of this scheme is that both power and control circuits are d.c and there is no isolation between the two.

* Another disadvantage is that a continuous d.c signal has to be applied. So gate power loss is high.

(ii) A.C gate triggering :-

* Here a.c source is used for gate signals.

* This scheme provides proper isolation between Power and control circuit.

* Drawback of this scheme is that a seperate transformer is required to step down ac supply.

(iii) Pulse gate triggering :-

* In this method the gate drive consists of a single pulse appearing periodically (or) a sequence of high frequency pulses.

* This is known as carrier frequency gating.

* A pulse transformer is used for isolation.

* The main advantage is that there is no need of applying continuous signals, so the gate losses are reduced.

Methods of turning OFF SCR:-

* Commutation is defined as the proces of turning OFF a SCR.

* In all commutation techniques, a reverse voltage is applied across the thyristor during the turn OFF proces.

* By turning OFF a thyristor we bring it from forward conducting to the forward blocking mode.

The conditions to be satisfied in order to turn OFF an SCR are:-

(i) $I_a < I_H$ (Anode current must be less than holding current).

(ii) A reverse voltage is applied to SCR for sufficient time enabling it to recover its blocking state.

There are two methods by which a thyristor can be commutated.

* Natural Commutation.
* Forced commutation.

NATURAL COMMUTATION:-

* In a.c circuit, the current always passes through zero every half cycle.

* As the current passes through natural zero, a reverse vge will simultaneously appear across the device. This will turn OFF the device immediately.

* This process is called as natural commutation, since no external circuit is required for this purpose.

FORCED COMMUTATION:-

* To turn OFF a thyristor, the forward anode current should be brought to zero for sufficient time to allow the removal of charged carriers.

* In case of d.c circuits the forward current should be forced to zero by means of some external circuits.

* This process is called as forced commutation.

Merits of SCR:-

* SCRs with high voltage and current ratings are available.
* ON state losses in SCRs are reduced.
* Very small amount of gate drive is required since SCR is a regenerative device.

Demerits of SCR:-

* Gate has no control after the SCR is turned ON.
* External circuits are required to turn OFF the SCR.
* Operating frequencies are very low.
* Snubber circuits are required for $\frac{dv}{dt}$ protection.

Applications of SCR:-

* SCRs are used for controlled rectifiers.
* AC regulators, lighting and heating applications.
* Dc motor drives, large power supplies and electronic circuit breakers.

SCR RATINGS:-

The values of Vge, current and switching frequencies of the SCRs, which when exceeded will damage the device are specified by the manufacturer.

Current ratings:-

a) Average current rating (I_T):-

It is the maximum repetitive average current that can flow through the SCR.

b) RMS current rating (I_{TR}):-

The rms current rating is the maximum repetitive rms current that can flow through the SCR.

c) Surge current rating (I_{TSM}):-

It is the peak amplitude of the surge current that the SCR can withstand only limited number of times in its life cycle. Surge current is normally specified as number of cycles and of peak amplitude.

d) i^2t rating:-

It is the measure of thermal energy that the device can absorb for a short period of time. Thermal energy is generated in the device due to fault occurence. The fuse clears the fault and protects the device. Fuse must clear the fault before the device is damaged due to exceeding i^2t rating.

e) $\frac{di}{dt}$ rating:-

The $\frac{di}{dt}$ rating specifies the maximum allowable rate of change of current through the device.

Voltage Ratings :-

a) Peak repetitive forward blocking voltage (V_{DRM}) :-

This is the maximum voltage that the SCR can block in the forward direction. If this rating is exceeded the device turns ON.

b) Peak repetitive reverse voltage (V_{RRM}) or Peak inverse vge (PIV) :-

This is the maximum voltage that the device can withstand repetitively in the reverse blocking state. The device is damaged when this rating is exceeded.

c) Non repetitive peak reverse voltage (V_{RSM}) :-

This is the maximum transient voltage that the device can safely withstand in the reverse direction. This transient is not repetitive.

d) $\frac{dv}{dt}$ rating :-

It specifies the maximum allowable rate of change of forward voltage that the device can withstand in forward direction.

If forward vge variations exceed $\frac{dv}{dt}$ ratings, the device turns ON.

FINGER VOLTAGE:

The minimum anode to cathode (V_{AK}) voltage that is to be applied across the SCR when the gate signal is applied for turning it ON is called finger vge.

Switching characteristics (or) Dynamic characteristics :-

Turn ON mechanism :-

* When a positive gate signal is applied to a forward biased SCR, the transition of SCR from blocking state to conducting state is called as turn ON mechanism.

* The time taken for SCR to traverse from the blocking state to conducting state is called as turn ON time.

* Turn On time is divided into 3 periods

$$t_{ON} = t_d + t_r + t_p$$

t_d = delay time ; t_r = rise time ; t_p (or) t_s = peak time (or) spread time.

* When the gate current reaches $0.9 I_G$ the anode current (I_A) starts increasing, and reaches $0.1 I_A$ (10% of its max value)

* The time taken for anode current to ↑ and reach $0.1 I_A$ is called as delay time (t_d). [or] It is the time taken for anode voltage to fall from V_A to $0.9 V_A$ is called as delay time.

* The anode current further increases and reaches $0.9 I_A$.

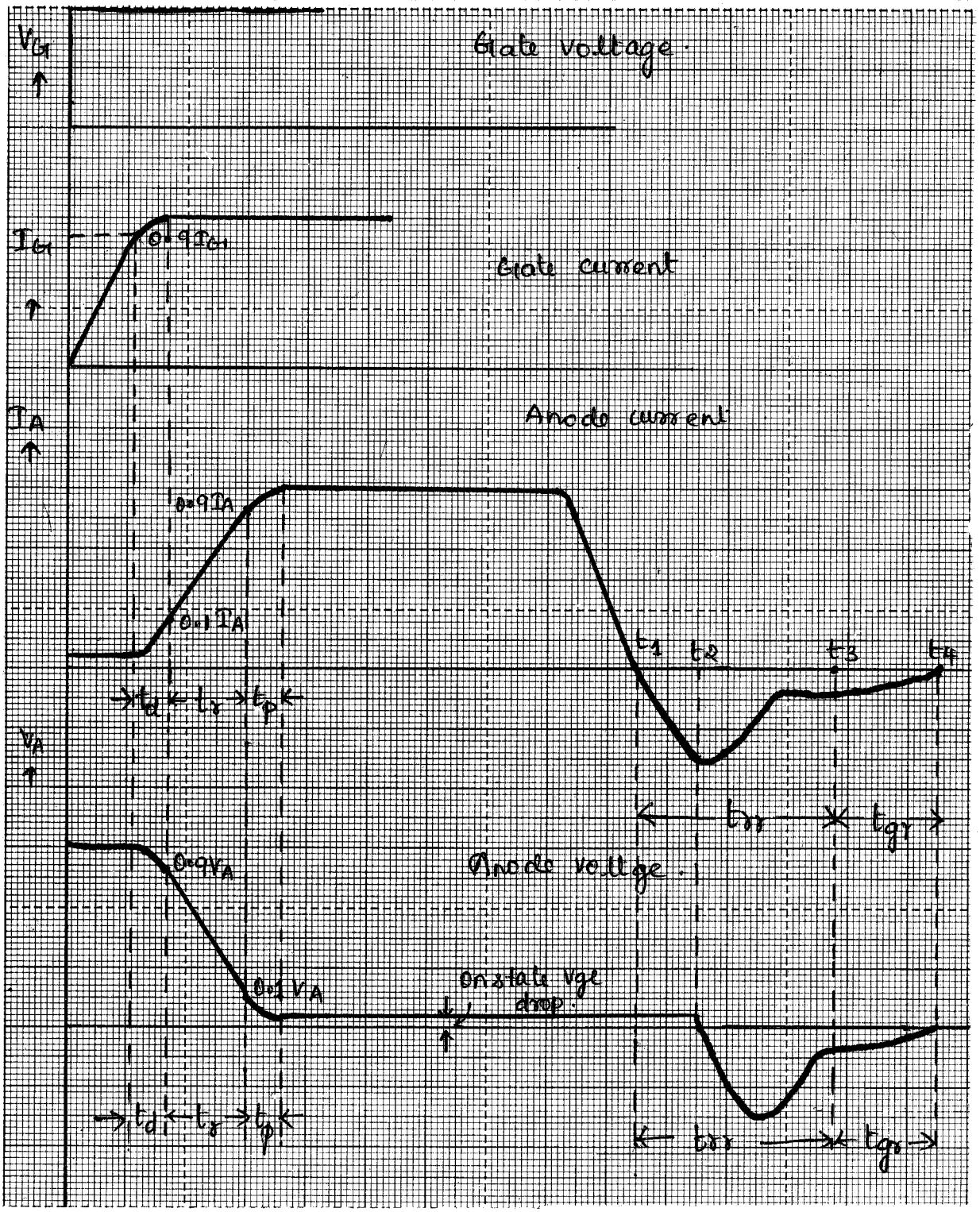
* The time taken by the anode current to increase from $0.1 I_A$ to $0.9 I_A$ is called as rise time (t_r). [or] it is the time taken by the anode voltage to fall from $0.9 V_A$ to $0.1 V_A$.

Spread time or peak time (t_s or t_p) :-

It is time taken by the anode current to rise from [$0.9 I_A$ to maximum value of I_A] 90% to 100% of its full value. (or) it is the time taken by V_A to fall

from $0.1V_A$ to its ON state voltage drop (nearly zero).

* During this time the conduction spreads over the entire cross section of cathode and so e^{-s} spread over all the junctions.



Turn OFF mechanism:

* Turning OFF an SCR means bringing the SCR from conducting state to blocking state.

* To turn OFF an SCR two things are to be done.

(i) Reduce the anode current below its holding current level.

(ii) Application of reverse voltage.

* When the anode current is zero, if we apply forward vge to the SCR, the device will not be able to block this forward vge due to the fact that excess charge carriers are still at the junctions, so the device will start conducting even when the gate signal is not applied.

* In order to avoid this, reverse biasing of SCR is done to remove the excess charge carriers from all four layers.

* The turn OFF time is defined as the time from the instant the anode current becomes zero to the instant SCR reaches its forward blocking ability.

turn off time $t_{OFF} = t_{rr} + t_{gr}$

t_{rr} = Reverse recovery time.

t_{gr} = Gate recovery time.

Reverse recovery proces is the removal of excessive charge carriers from the top and bottom layers of SCR.

* At t_1 ; current $I_A = 0$.

* After t_1 ; I_A build up in the reverse direction, due to the charge carriers stored in the four layers.

* Reverse recovery current removes the excesive carriers from junctions J_1 and J_3 during the time t_1 to t_3. (Reverse recovery current flows due sweeping out of holes from top p-layer and e^{s} from bottom n-layer)

Reverse recovery time :- t_{rr}

It is the time taken for the removal of excesive carriers from top and bottom layer of SCR.

* At t_2 ; when nearly 60% of charges are removed from the outer two layers, the reverse recovery current (I_{rev}) decays.

* This decaying causes a reverse V_{GK} to be applied across the SCR.

* At t_3 all excesive carriers from J_1 and J_3 is removed.

* The reverse voltage across SCR removes the excesive carriers from function J_2.

* Gate recovery process is the removal of excesive carriers from J_2 junction by application of reverse V_{GK}.

* Time taken for removal of trapped charges from J_2 is called gate recovery time. (t_{gr}).

* At t_4 all the carriers are removed and the device moves to the forward blocking mode.

THYRISTOR PROTECTION :-

* For reliable operation of SCR, it should be operated within the specific ratings.

* SCRs are very delicate devices and so they must be protected against abnormal operating conditions.

* various protections of SCR are.

a) $\frac{di}{dt}$ protection. b) $\frac{dV}{dt}$ protection.

c) over voltage protection d) over current protection.

a) $\frac{di}{dt}$ protection:-

* $\frac{di}{dt}$ is the rate of change of current in a device.

* when SCR is forward biased, and is turned ON by the gate signal the anode current flows.

* The anode current requires some time to spread inside the device. (to spread the charge carriers)

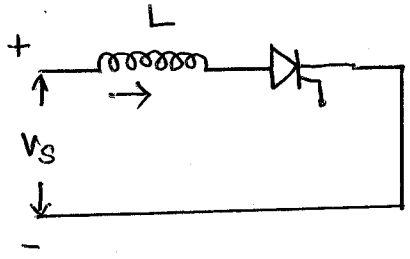
* But if the rate of rise of anode current $\left(\frac{di}{dt}\right)$ is greater than the spread velocity of charge carriers then local hot spots is created near the gate due to increased current density. This localised heating may damage the device.

* Local spot heating is avoided by ensuring that the conduction spreads to the whole area very rapidly.

(or)

* The $\frac{di}{dt}$ value must be maintained below a limiting value.

* This is done by means of connecting an inductor in series with the thyristor.



* The inductance L opposes the high $\frac{di}{dt}$ variations.

* when the current variation is high, the inducts smooths it and protects the SCR from damage.

(Though $\frac{di}{dt}$ variation is high, "L" smooths it because it takes some time to charge].

$$L \geq \frac{V_S}{\left(\frac{di}{dt}\right)}$$

b) $\frac{dv}{dt}$ protection:-

* $\frac{dv}{dt}$ is the rate of change of voltage in SCR.

* we know that $i_c = C \cdot \frac{dv}{dt}$ [already discussed in $\frac{dv}{dt}$ triggering] Page NO: 94

∴ when $\frac{dv}{dt}$ is high, i_c is high.

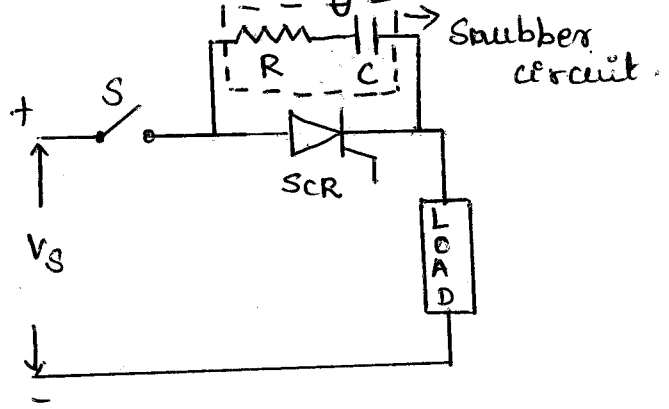
This high current may turn ON SCR even when gate curr is zero.

This is called as $\frac{dv}{dt}$ turn ON (or) false turn ON of SCR.

* To protect the SCR against false turn ON (or) against high $\frac{dv}{dt}$ a SNUBBER CIRCUIT is used.

SNUBBER CIRCUIT:-

* It is a series combination of resistor and capacitor.
* They are connected across the thyristor to be protected.
* The capacitor 'C' is used to limit the $\frac{dv}{dt}$ across the SCR.
* The resistor 'R' is used to limit high discharging current through the SCR.



* when switch S is closed, the capacitor 'C' behaves as a short circuit.
* ∴ Vge across SCR = 0.
* As time ↑es; Vge across 'C' ↑ at a slow rate.
* ∴ $\frac{dv}{dt}$ across 'C' and SCR is less than maximum $\frac{dv}{dt}$ rating of the device.
* The capacitor charges to full Vge V_S; after which gate is triggered, and SCR is turned ON and high current flows through SCR.
* ∴ $\frac{di}{dt}$ is high and may damage SCR. So the resistor R in series with 'C' will limit the magnitude of $\frac{di}{dt}$.

i.e $\frac{V_S}{R_S}$ is ↓ so $\frac{di}{dt}$ is ↓

c) Over voltage protection:

*Over voltage may result in false turn ON of the device (or) damage the device.

* SCR is subjected to internal and external over voltage.

Internal overvoltage:-

The reverse recovery current decays at a very fast rate ($\frac{di}{dt}$). So a voltage surge = $L\frac{di}{dt}$ is produced.

External over voltage:-

These are caused due to interruption of current flow in the inductive circuit and also due to lightning strokes on the lines feeding the SCR systems.

The effect of overvoltage is reduced by using Snubber circuits and non linear resistors called VOLTAGE CLAMPING DEVICES.

[Protection by snubber circuit is already discussed].

Snubber ckt provide partial protection.

Voltage clamping device:- (V.C)

* It is a non-linear resistor (VARISTOR) connected across the SCR

* The V.C has falling resistance chs with ↑ing vge.

* During normal operation V.C has high R and draws only small leakage current.

* when high vge appears, V.C operates in low Resistance region, and the surge energy is dissipated across the resistance by producing a virtual S.C across the SCR.

d) Over current protection:-

* In an SCR, due to over current the junction temperature exceeds the rated value and the device gets damaged.

* Over current is interrupted by conventional fuses (current limiting fuse) C.L. fuse. and circuit breakers.

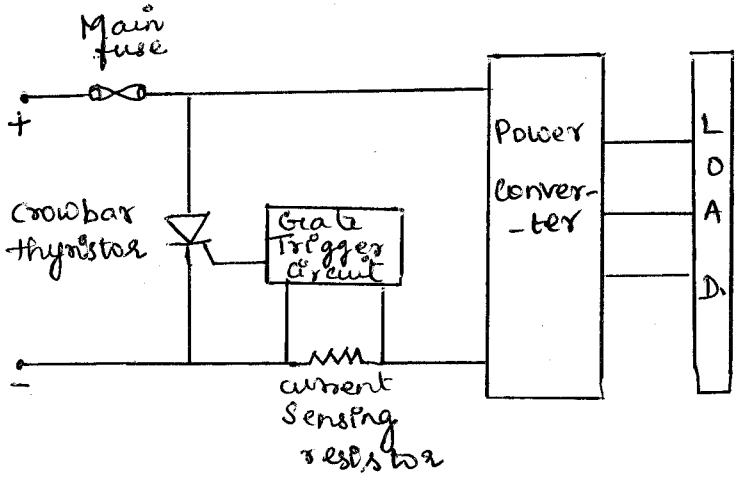
* The fault current must be interrupted before the SCR is damaged and only the faulty branches of the n/w should be isolated.

* Circuit breaker has long tripping time. So it is used for protecting SCR against continuous over loads (or) against surge currents of long duration.

* Fast acting current limiting fuse is used to protect SCR against large surge currents of very short duration.

ELECTRONIC CROWBAR PROTECTION:-

* SCR has high surge current ability
* SCR is used in electronic crowbar circuit for over current protection of power converter.
* SCR is connected across the supply.



* Current sensing resistor detects the value of converter current.
* If it exceeds preset value, then gate trigger circuits turns ON the crowbar SCR.
* So the i/p terminals are S.C by SCR and it shunts away the converter over current.
* After some time main fuse interrupts the fault current.

TRIGGERING CIRCUITS OF SCR: (or) FIRING CIRCUITS

The process of giving gate pulse to the SCR is called as Firing (or) triggering.

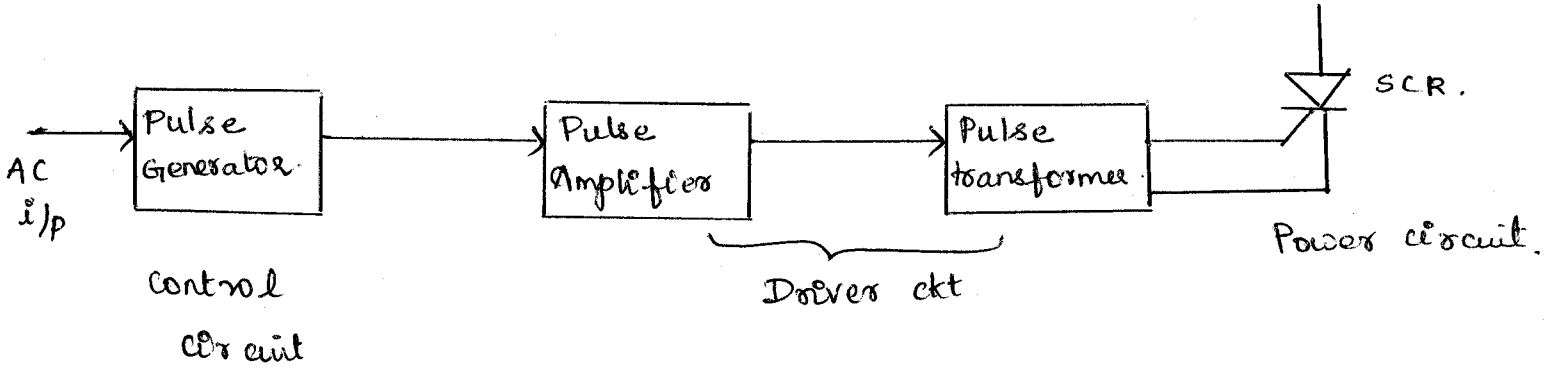
Current applied to gate should be of

* Sufficient amplitude and short rise time.
* Sufficient duration
* Occur at time when main circuit conditions are favourable to conduction.

Longer pulse duration is required because of the following reason:

* A relatively long period may be required for the anode current to rise to anode current level.
* Oscillation or other disturbances may conspire to turn off the thyristor shortly after it is first triggered.
* There may be uncertainity as to whether the anode circuit conditions are favourable to conduction when the firing pulse is initiated.
* Firing circuit must produce triggering pulse for every SCR at proper instant.

General layout of firing scheme:



* Triggering pulses generated by the control circuit need to be amplified and passed through isolation circuits.

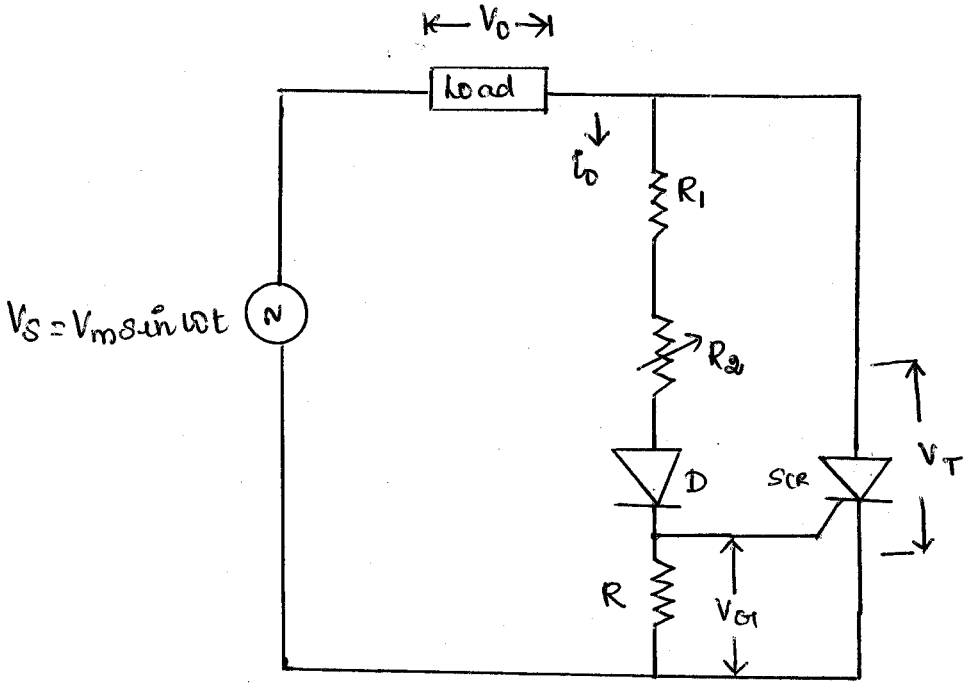
* Trigger pulses have very small power, so they must be amplified by amplifier.

* Firing circuit operate at low level (5 - 20 V) and SCR at high (> 250V) it Vge level. ∴ Isolation between them is required and is provided by pulse transformer.

Types of triggering circuits :-

1. Resistance triggering.
2. Resistance - Capacitance triggering.
3. Uni Junction transistor (UJT) triggering.

1. RESISTANCE TRIGGERING :-



R_1 = limiting resistor.

R_2 = Variable resistance.

R = stabilising resistance.

The functions of the various components are disussed below.

R_1 :- (limiting resistor)

* If R_2 is very less or equal to zero. then the current I_g will flow from. Source → Load → R_1 → D → Gate to cathode of SCR.

* This current I_g should not exceed max permissible gate current. (I_{gm}). ∴ $R_1 \geq \frac{V_m}{I_{gm}}$ (V_m = maximum source voltage).

∴ R_1 should limit gate current when R_2 is varied.

R :- (stabilising resistance).

* when current flows through R, a vge drop V_G appears across it and is applied between the gate and cathode of SCR.

* This vge V_G should not exceed the maximum possible gate voltage V_{gm}. ∴ R should be of such a value to limit V_G below V_{gm}.

∴ $R \leq \frac{V_{gm} \cdot R_1}{V_m - V_{gm}}$ (when $R_2 = 0$).

$$V_{gm} = \frac{V_m * R}{R_1 + R}$$

$$\therefore R = \frac{V_{gm} R_1}{V_m - V_{gm}}$$

diode D :-

* Diode is a unidirectional device. It conducts only in the forward biased condition.

* It is used to prevent the SCR's (V_{GK}) reverse bias vge from exceeding peak reverse vge. during -ve half cycle.

* Diode allows flow of current in +ve half cycle only * ∴ gate vge V_G is half wave dc pulse. Amplitude of this dc pulse is controlled by varying R_2.

V_{GP} = Peak value of gate voltage

V_{GT} = Gate trigger voltage.

$V_G = i_o R$.

$$V_{GP} = \frac{V_m \cdot R}{R_1 + R_2 + R}$$

* If R_2 is high, current flowing is less; $\therefore$ Vge drop across R is less i.e. V_G is ↓ and so peak value of V_G is also less. i.e., V_{GP} is ↓.

* If R_2 is ↓; i_o ↑; $\therefore V_G = i_o R$ ↑; $\therefore$ peak value V_{GP} ↑.

* If V_{GP} is less than V_{GT}; SCR will not turn ON.

* <u>R_2 decides the firing angle α</u>. It is the angle (or) the instant at which the SCR turns ON.

$$V_{GP} \sin\alpha = V_{GT}$$

$$\sin\alpha = \frac{V_{GT}}{V_{GP}}$$

$$\alpha = \sin^{-1}\left(\frac{V_{GT}}{V_{GP}}\right) = \sin^{-1}\left(\frac{V_{GT}}{\frac{V_m \cdot R}{R_1+R_2+R}}\right)$$

$$\therefore \alpha = \sin^{-1}\left[\frac{V_{GT} * (R_1+R_2+R)}{V_m \cdot R}\right]$$

$\because$ V_m, R, R_1, V_{GT} are constant.

$$\alpha \propto \sin^{-1}(R_2)$$

(or) $\alpha \propto R_2$

$\therefore$ as R_2 ↑ α ↑

* In R triggering the firing angle can be varied only between $0-90^\circ$, because

$V_s = V_m \sin\theta$; at $\theta = 90^\circ$

$V_s = V_m$ = max value.

∴ V_{GT} will occur somewhere below 90° and not after that.

Case (i) $V_{GP} < V_{GT}$.

If R_2 is adjusted to a high value then $R_2 \uparrow$; $i_o \downarrow$; $V_G = i_o R \downarrow$ ∴ $V_{GP} \downarrow$. If V_{GP} is $< V_{GT}$ then SCR will not turn ON. Also here $\left[\alpha = \sin^{-1}\left(\frac{V_{GT}}{V_{GP}}\right)\right]$. Only when it crosses V_{GT} SCR will turn ON. ∴ $i_o = V_o = 0$. and V_{ge} across SCR V_T follows V_s.

Case (ii) $V_{GP} = V_{GT}$. $(\alpha = 90^\circ)$

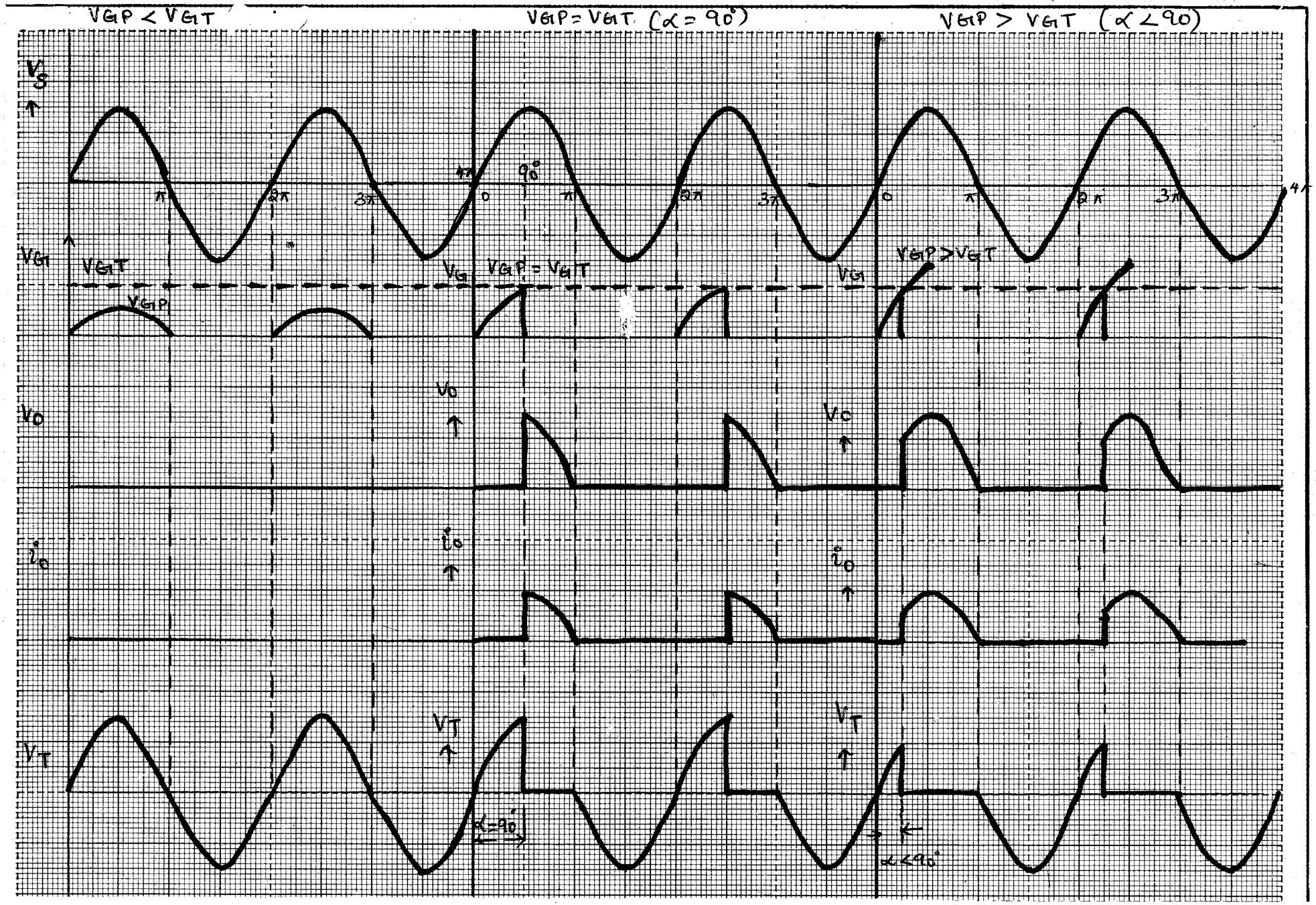
* If R_2 is adjusted such that $V_{GP} = V_{GT}$ then $\alpha = \sin^{-1}\left(\frac{V_{GT}}{V_{GP}}\right) = 90^\circ$. i.e V_{GP} will be equal to V_{GT} at 90° and SCR will turn ON at 90°. Till then it will be OFF. After $\alpha = 90^\circ$, V_o and i_o will flow.

* When SCR turns ON V_{ge} across SCR $V_T = 0$.

* ONCE SCR is ON gate is removed.

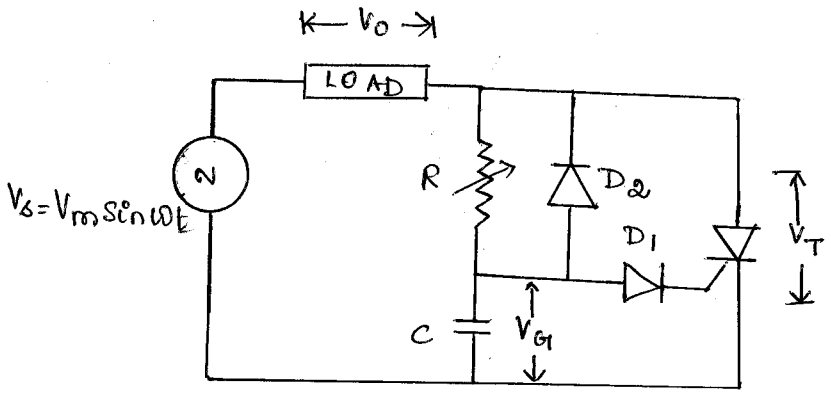
Case (iii) $V_{GP} > V_{GT}$ $(\alpha < 90^\circ)$

* If R_2 is adjusted so that V_{GP} is $> V_{GT}$ then α will be less than 90°. So SCR will turn ON at the instant when V_{GP} reaches V_{GT} first. at some angle $\alpha < 90^\circ$.


VGP < VGT
VGP = VGT (α = 90°)
VGP > VGT (α < 90)
VS
VG
VGT
VGP
VO
iO
VT
π
2π
3π
4π
0
90°
α = 90°
α < 90°

2. RESISTANCE - CAPACITANCE TRIGGERING:-

(i) R-C Half wave trigger circuit :-



* Firing angle can be controlled from 0 to 180° by varying R.

In Negative half cycle:

* In -ve half cycle, the SCR and diode D_1 is reverse biased and so it does not conduct.

* But the diode D_2 is forward biased and so the the capacitor 'C' charges on the negative side through diode D_2.

At this period SCR is OFF.

∴ Voltage and current across load = 0

i.e $V_o = i_o = 0$.

∴ V_{ge} across SCR $V_T = V_s$.

In positive half cycle:-

In +ve half cycle SCR is forward biased through diode D_1.

At $t = 0$, $V_T = V_s$.

If the value of R is high the capacitor charges very slowly.

* If value of R is less capacitor charges very fast.

* voltage across the capacitor appears across the gate - cathode of SCR through diode D_1.

* when gate voltage $V_G = V_{GT}$ (gate trigger voltage) SCR turns ON.

So when $V_C = V_{GT} + V_{d_1}$ SCR turns ON.

V_{d_1} = Vge drop across diode.

If drop across diode is neglected $V_C = V_{GT}$.

Case(i)

If R is high the current i_0 is less and capacitor will charge very slowly to final value. So V_C will be equal to V_{GT} after a very long time and so SCR will turn ON at a large firing angle α. So R↑, α↑. ($R \propto \alpha$)

Case(ii)

If R is less, i_0 is high, capacitor will charge very fast and V_C will be equal to V_{GT} fast. So SCR will turn ON at a small firing angle. so R↓, α↓

$$R \leq \frac{V_s - V_{GT} - V_{d_1}}{I_{gt}}$$

I_{gt} = Gate trigger current.

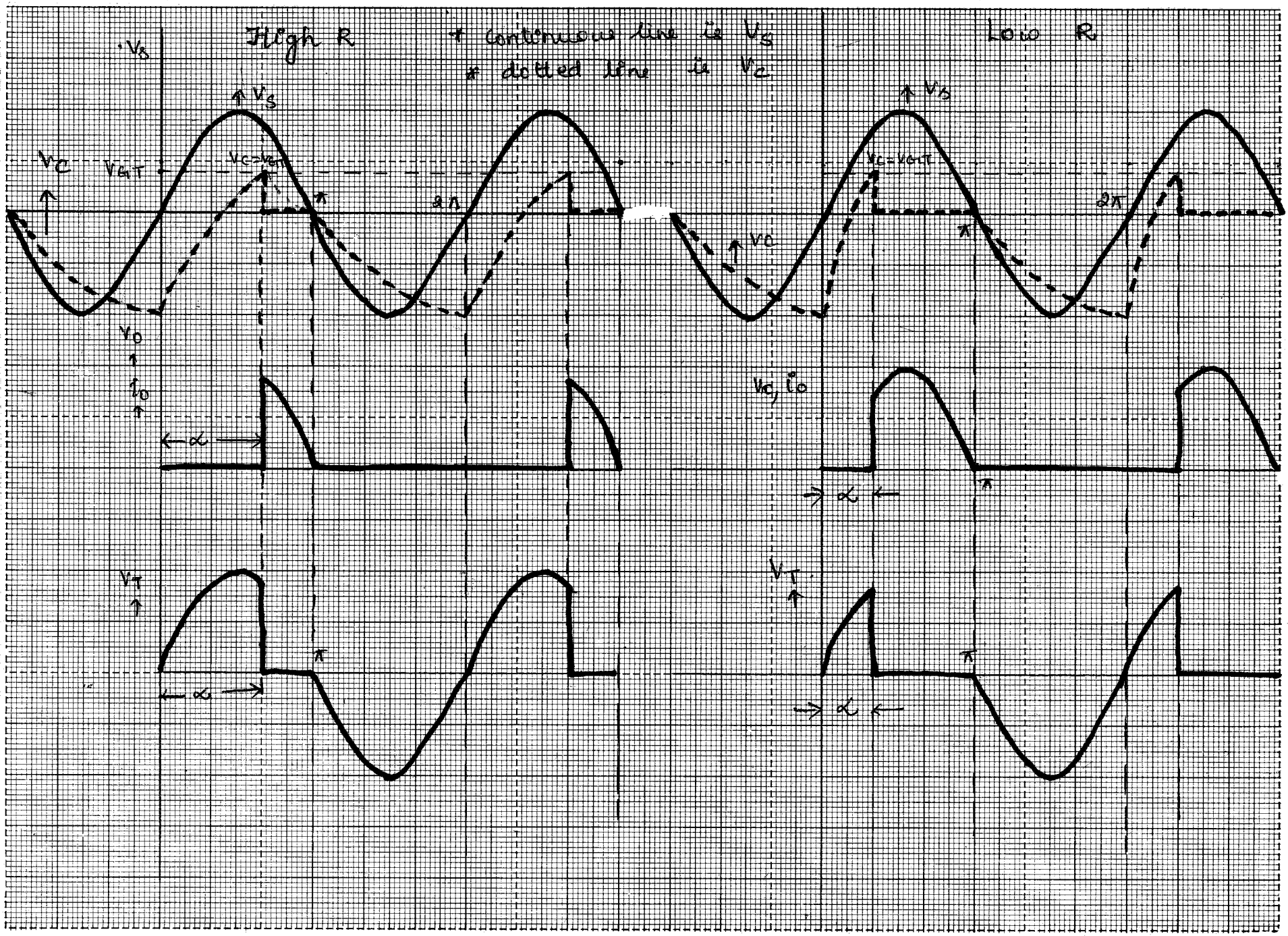
So at α when $V_C = V_{GT}$ SCR will turn ON.

So at $t = \alpha$, SCR is ON

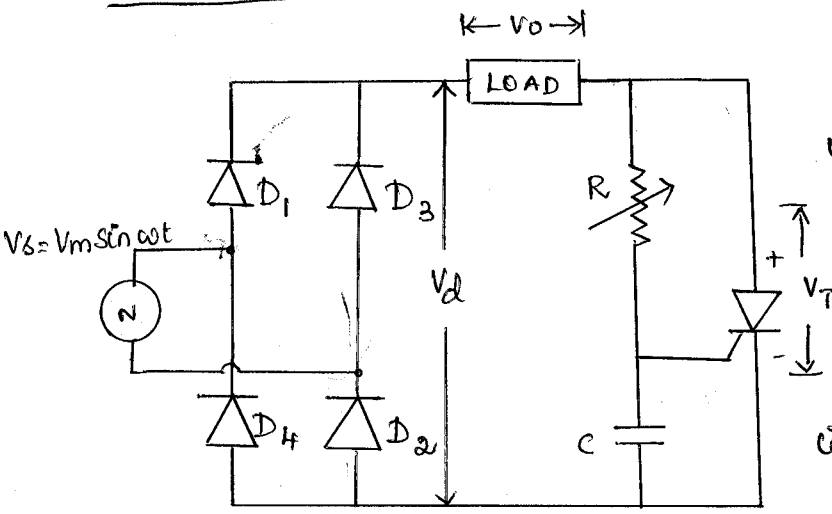
Vge across SCR $V_T = 0$

Vge across load $V_0 = V_s$

When SCR is ON Vge across capacitor V_C will discharge and reach Zero.


High R
* continuous line is V_S
# dotted line is V_C
Low R
V_S
V_C
V_{GT}
$V_C > V_{GT}$
2π
π
V_o
i_o
α
V_T

(ii) RC full wave trigger circuit :



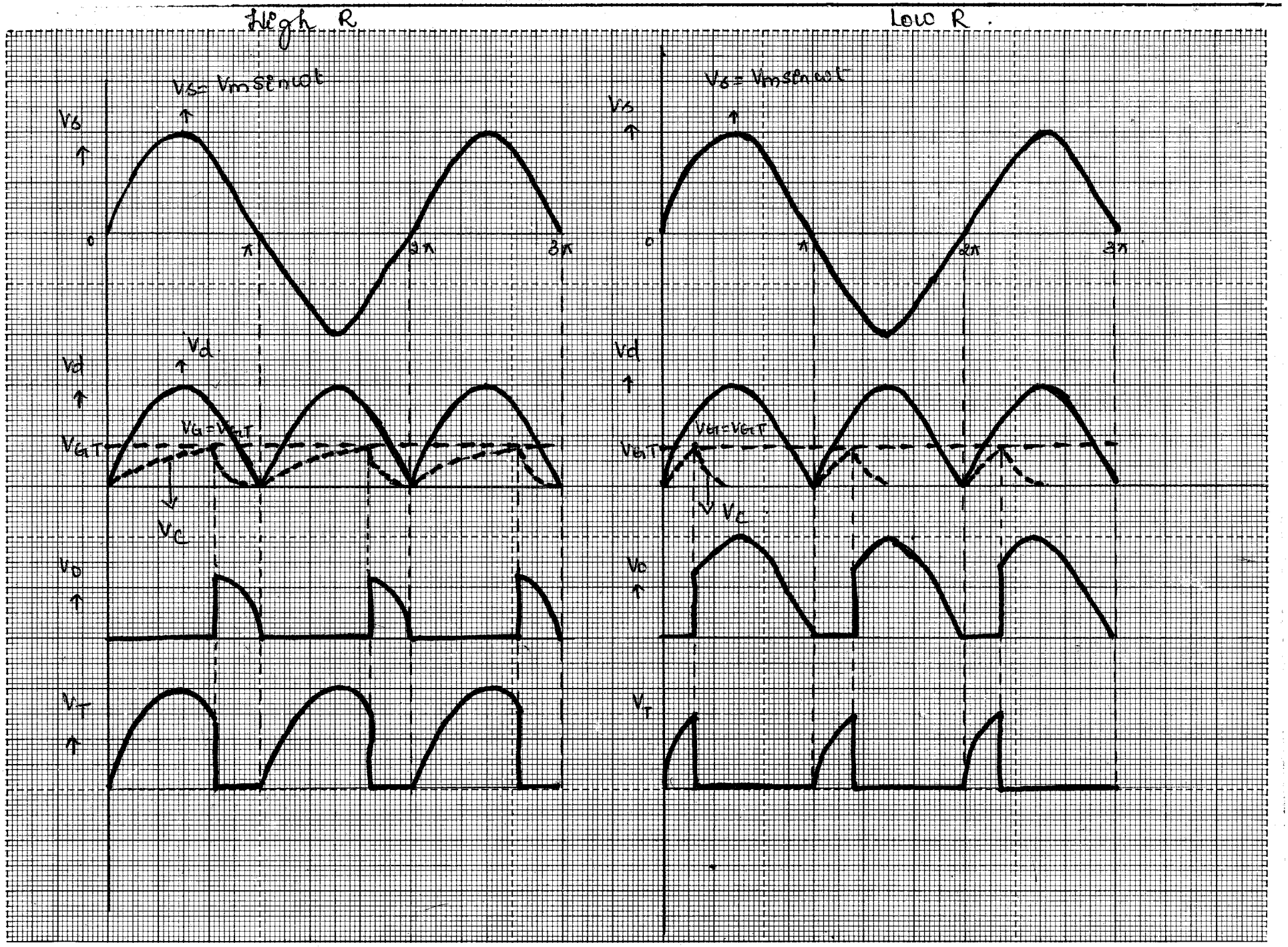
* Supply is given to full wave diode bridge rectifier.
* The rectified vge is given to the SCR.
* O/p of rectifier is dc i.e., only +ve half cycles.

Case(i) If value of R is high ; i_o is less. The capacitor C will charge slowly. The capacitor vge is fed across the gate and cathode of thyristor. when the $V_G = V_{GT}$ SCR will turn ON. When R is high the capacitor charges slowly and reaches V_{GT} very slowly. So α is high. When SCR turns ON the vge across the thyristor is zero and vge across capacitor is also zero. (since it discharges)

Case(ii) If value of R is low ; I_o is high. Capacitor C will charge fast. The capacitor vge V_C will reach V_{GT} fast. So at $V_G = V_{GT}$ SCR will turn ON. So for less R, α is also less.

* Rectifier converts ac to dc.
* At $V_G = V_{GT}$ SCR is ON. (ie at $t = \alpha$) $V_o = V_d$.
* At ON state ; $V_T = 0$
* At $t=0$; SCR is OFF ; $V_T = V_d$, $V_o = 0$.

$$R \leq \frac{V_s - V_{GT}}{I_{gt}}.$$


High R
Low R.
$V_S = V_m \sin \omega t$
V_S
V_d
V_{GT}
$V_G = V_{GT}$
V_C
V_D
V_T
0
π
2π
3π

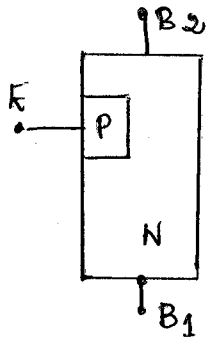
3. UJT TRIGGERING:-

UJT:- Uni Junction transistor.

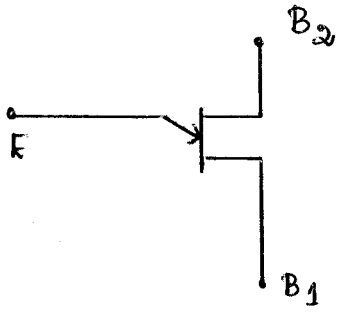
CONSTRUCTION:-

* It is made of n-type silicon base to which P-type emitter is embedded.

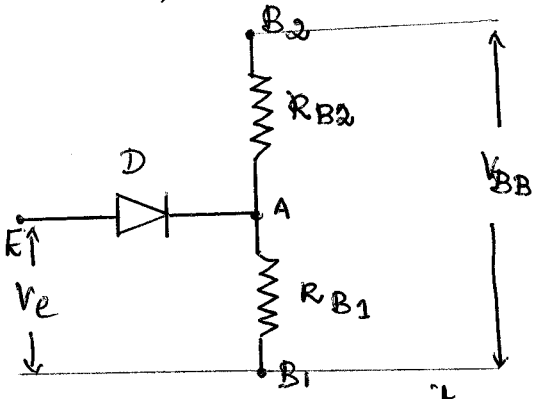
* It has 3 terminals - Emitter [E]; base-one [B_1]; base-two [B_2].



construction.



symbol



equivalent circuit.

EQUIVALENT CKT:-

* R_{B1} and R_{B2} are the internal resistances from bases B_1 and B_2 to point A.

* when a voltage V_{BB} is applied across B_1 and B_2 Vge across point A and B_1 is given as follows.

$$V_{AB_1} = V_{BB} * \frac{R_{B_1}}{R_{B_1}+R_{B_2}} = \eta \cdot V_{BB}.$$

$$\therefore V_{AB_1} = \eta \cdot V_{BB}$$

where $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}$ = Intrinsic stand off ratio.

WORKING:-

* when V_{BB} is applied, emitter diode D is reverse biased due to Vge drop across R_{B1} i.e., $V_{AB_1} = \eta \cdot V_{BB}$.

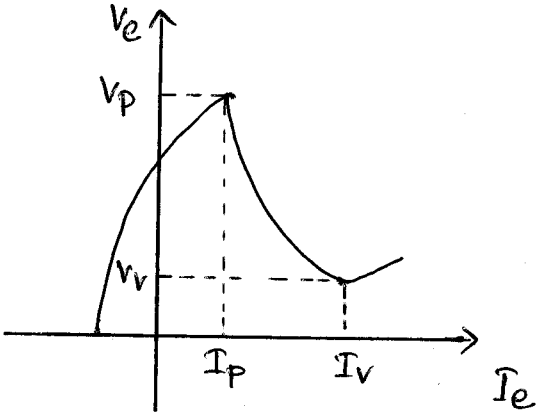
* Now when emitter Vge Ve is applied between E and B_1, the diode remains reverse biased till $V_e < \eta V_{BB} + V_D$.

* So emitter current is negative. V_D = Vge drop across diode.

* when $V_e = \eta V_{BB} + V_D$, the E-B_1 junction is forward biased and it begins to conduct. So I_e is positive. This value of emitter voltage which causes the diode to conduct (or) UJT to conduct is called peak point voltage (Point B).

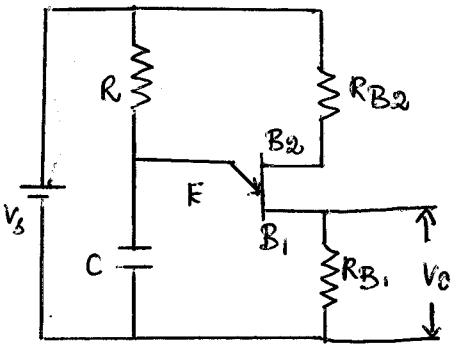
$\therefore V_p = \eta V_{BB} + V_D$.

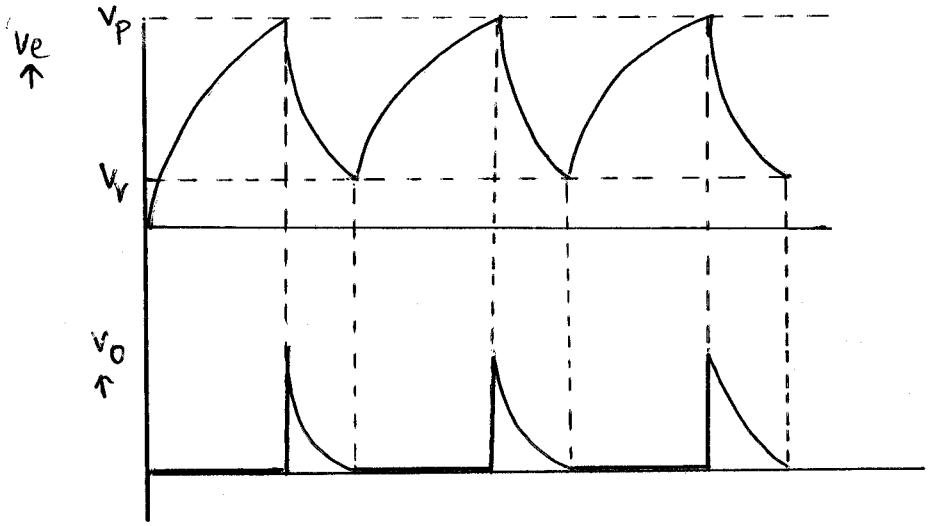
* when UJT turns ON, the cunt I_e ↑ and V_{ge} across the device V_e ↓. V_{ge} decreases till a voltage called as valley V_{ge} (V_v). After V_v the device is in saturation region. When V_{ge} reaches V_v device turns OFF.



UJT CHARACTERISTICS

UJT RELAXATION OSCILLATOR (OR) UJT TRIGGERING:



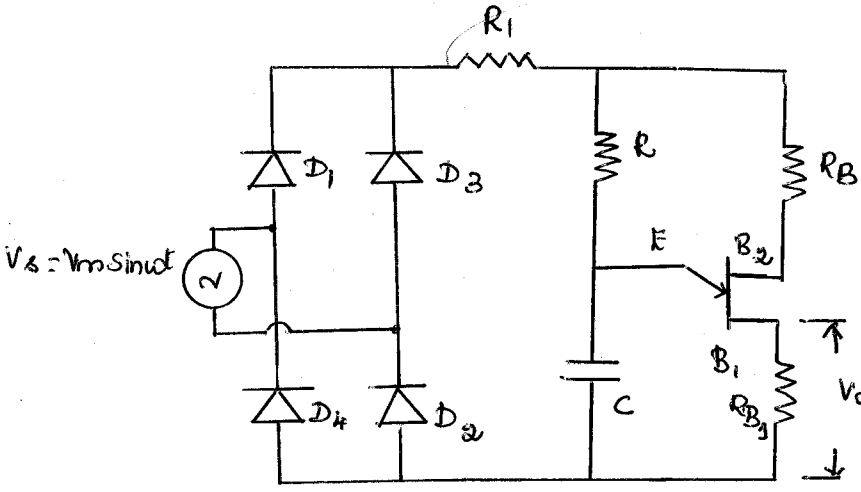


* Capacitor C charges through R. V_{ge} across capacitor is applied across emitter.

* when $V_c = V_e = V_p$ UJT is ON. Capacitor discharges through UJT. through $R_{B1} = V_o$.

* when V_c falls to valley vge V_v the device is OFF. So during every instant UJT is ON, the capacitor discharges through R_{B1} so vge is available across O/P.

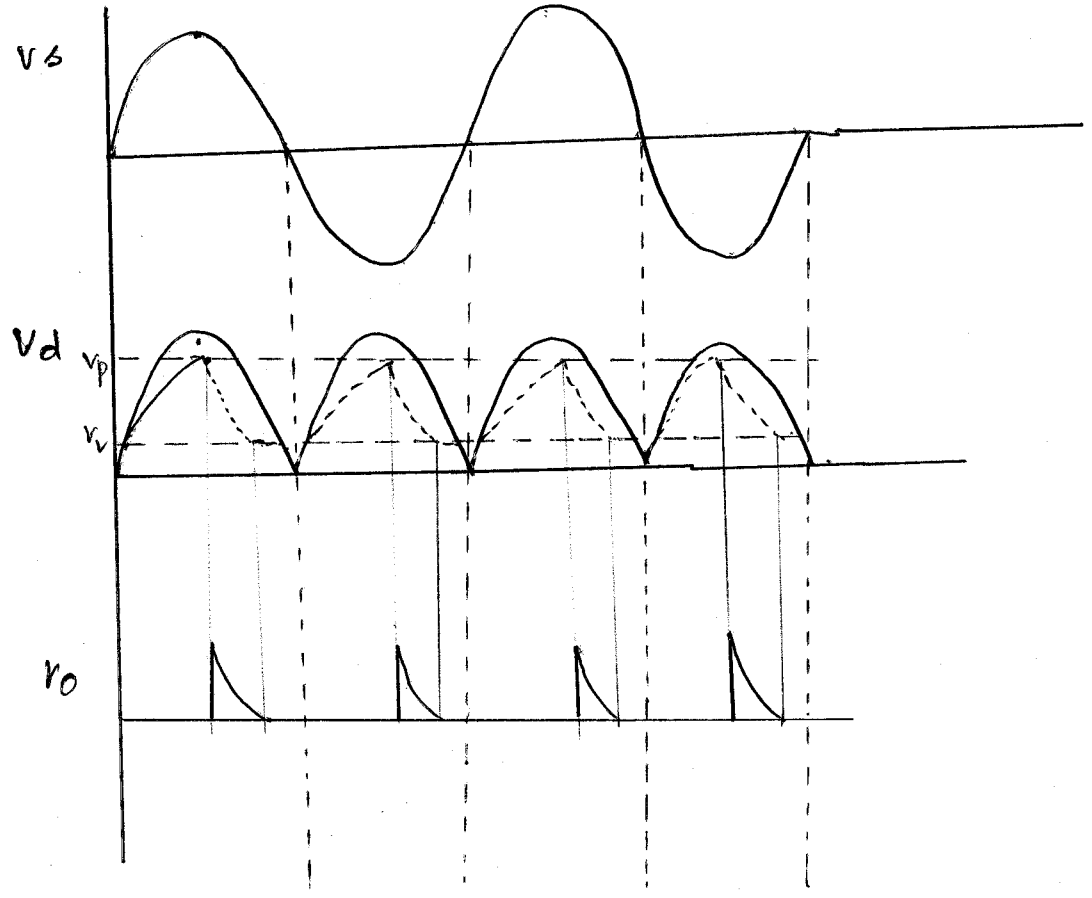
SYNCHRONISED UJT TRIGGERING OR RAMP TRIGGERING:



* The UJT is fed with rectified dc vge.
* Capacitor C charges through R
* when $V_c = V_p$ (peak vge) UJT is ON.

* So when UJT is ON capacitor discharges thro' R_{B1}.

* As V_c ↓ and reached a valley vge (V_v) the device turns OFF and again capacitor charges thro' R.



COMMUTATION TECHNIQUES:

The process of turning OFF an SCR is called as commutation. SCR can be turned OFF by

(i) applying a reverse voltage

(ii) bringing the anode current level below the holding current level.

a) Natural commutation:-

If the type of supply available is A.C, naturally after every half cycle voltage across SCR will be reversed making the anode current to fall below holding current level, thereby turning it OFF.

b) Forced commutation:-

If the type of supply available is d.c. it is not possible to reverse in order to turn OFF an SCR. So forcibly it should be reversed for meeting the requirement by using energy storing elements like L and C.

Types of commutation:

a) Class - A commutation. (or) load commutation:

b) Class - B (or) Resonant pulse commutation.

c) class - C (or) Complementary Impulse commutation.

d) class - D (or) auxilary commutation

e) class - E (or) External pulse commutation.

f) class - F (or) line commutation.

Vge across capacitor $V_c = \frac{1}{C}\int_0^t i \cdot dt$

$\therefore V_c = \frac{1}{C}\int_0^t V_s \cdot \sqrt{\frac{C}{L}} \sin \omega_0 t \cdot dt$

$V_c = \frac{1}{C} \cdot V_s \cdot \sqrt{\frac{C}{L}} \int_0^t \sin \omega_0 t \cdot dt = \frac{1}{C} * V_s * \sqrt{\frac{C}{L}} \left[-\frac{\cos \omega_0 t}{\omega_0} \right]_0^t$

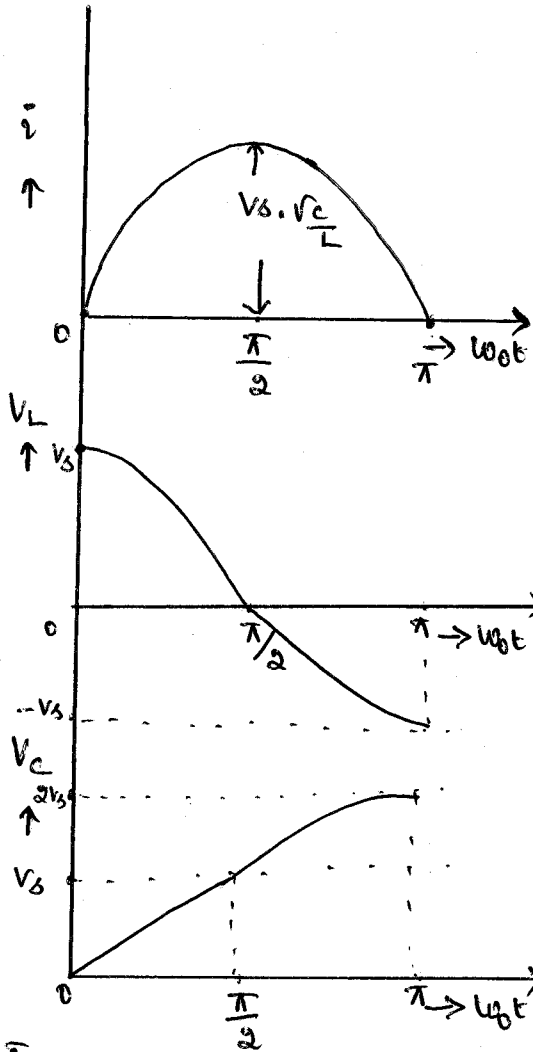
$V_c = -\frac{1}{C} * V_s * \sqrt{\frac{C}{L}} * \frac{1}{\omega_0} \left[\cos \omega_0 t \right]_0^t = -V_s * \sqrt{\frac{C}{L}} * \frac{1}{C} * \frac{1}{\frac{1}{\sqrt{LC}}} * \left[\cos \omega_0 t \right]_0^t$

$V_c = -V_s * \sqrt{\frac{LC^2}{LC^2}} * \left[\cos \omega_0 t - \cos 0 \right] = -V_s \left[\cos \omega_0 t - 1 \right]$

$\therefore \boxed{V_c = V_s (1 - \cos \omega_0 t)}$

Let us trace the waveforms for i, V_c, V_L.

	At $\omega_0 t = 0$	$\omega_0 t = \frac{\pi}{2}$	$\omega_0 t = \pi$
$i = V_s \cdot \sqrt{\frac{C}{L}} \cdot \sin \omega_0 t$	$i = 0$	$i = V_s \cdot \sqrt{\frac{C}{L}}$	$i = 0$
$V_L = V_s \cos \omega_0 t$	$V_L = V_s$	$V_L = 0$	$V_L = -V_s$
$V_C = V_s (1 - \cos \omega_0 t)$	$V_c = 0$	$V_c = V_s$	$V_c = 2V_s$



So we see that when $i = 0$ at $\omega_0 t = \pi$; SCR turns OFF.

This is also called as load or resonant commutation.

$\because \omega_0 = \frac{1}{\sqrt{LC}}$

$\omega_0^2 = \frac{1}{LC}$

On substituting in eqn ① we get

$$I(s) = \frac{V_s}{L} * \frac{1}{s^2 + \omega_0^2}$$

On multiplying and dividing by ω_0 we get

$$I(s) = \frac{V_s}{L} * \frac{\omega_0}{\omega_0} * \frac{1}{s^2 + \omega_0^2} = \frac{V_s}{\omega_0 L} * \frac{\omega_0}{s^2 + \omega_0^2}$$

Put $\omega_0 = \frac{1}{\sqrt{LC}}$

$$\therefore I(s) = \frac{V_s}{\frac{1}{\sqrt{LC}} * L} * \frac{\omega_0}{s^2 + \omega_0^2} = \frac{V_s}{\sqrt{\frac{L^2}{LC}}} * \frac{\omega_0}{s^2 + \omega_0^2}$$

$$I(s) = \frac{V_s}{\sqrt{\frac{L}{C}}} * \frac{\omega_0}{s^2 + \omega_0^2} = V_s * \sqrt{\frac{C}{L}} * \frac{\omega_0}{s^2 + \omega_0^2}$$

On taking inverse laplace transform we get

$$\boxed{i(t) = V_s \cdot \sqrt{\frac{C}{L}} \cdot \sin \omega_0 t}$$

Vge across inductor $= V_L = L \cdot \frac{di}{dt} = L \cdot \frac{d}{dt}\left[V_s \cdot \sqrt{\frac{C}{L}} \cdot \sin \omega_0 t\right]$

$$V_L = L * V_s * \sqrt{\frac{C}{L}} * \frac{d}{dt}\left[\sin \omega_0 t\right] = L \cdot V_s * \sqrt{\frac{C}{L}} * \cos \omega_0 t * \omega_0$$

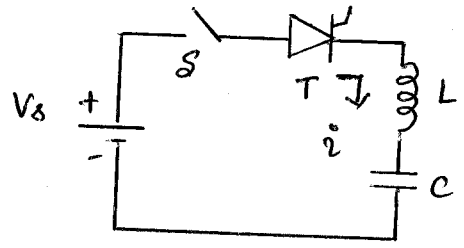
$$= V_s * L * \sqrt{\frac{C}{L}} * \omega_0 * \cos \omega_0 t \cdot \qquad \because \omega_0 = \frac{1}{\sqrt{LC}}$$

$$V_L = V_s \cdot \cos \omega_0 t * L * \sqrt{\frac{C}{L}} * \frac{1}{\sqrt{LC}} = V_s \cos \omega_0 t * \sqrt{\frac{L^2 C}{L^2 C}}$$

$$\therefore \boxed{V_L = V_s \cos \omega_0 t}$$

Let us see how the current decays to zero in such a circuit.

* let us consider an SCR fed with a constant dc Vge V_s and a switch S and 'L' and 'C'.



* when the switch S is closed the SCR T is forward biased.
* By giving a gate pulse the SCR is turned ON.

* when SCR turns ON current "i" starts flowing through it. Vge across SCR = 0.

∴ At t=0; when SCR turns ON, the Vge equation of the circuit is

$$V_s = V_L + V_C$$

$$V_s = L\cdot\frac{di}{dt} + \frac{1}{C}\int i\,dt.$$

Taking laplace.

$$\frac{V_s}{s} = L\cdot s\,I(s) + \frac{1}{C}\cdot\frac{I(s)}{s}$$

$$\frac{V_s}{s} = I(s)\left[Ls + \frac{1}{Cs}\right]$$

$$\frac{V_s}{s} = I(s)\left[\frac{LCs^2+1}{Cs}\right]$$

$$\therefore I(s) = \frac{\left(\frac{V_s}{s}\right)}{\left[\frac{LCs^2+1}{Cs}\right]} = \frac{V_s}{\cancel{s}} * \frac{C\cancel{s}}{LCs^2+1} = \frac{V_s * C}{LCs^2+1}$$

$$I(s) = \frac{V_s * \cancel{C}}{L\cancel{C}\left[s^2+\frac{1}{LC}\right]} = \frac{V_s}{L} * \frac{1}{\left(s^2+\frac{1}{LC}\right)} \rightarrow (1)$$

Resonant frequency $\omega_0 = \frac{1}{\sqrt{LC}}$

Note:-
When SCR is ON, Vge across SCR = 0 current flows.

V_L = Vge across L
V_C = Vge across C
[V_s is a constant dc Vge.
∴ $L[V_s] = \frac{V_s}{s}$]

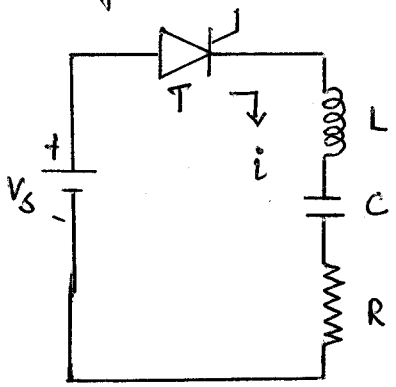
a) CLASS - A [or] LOAD COMMUTATION:

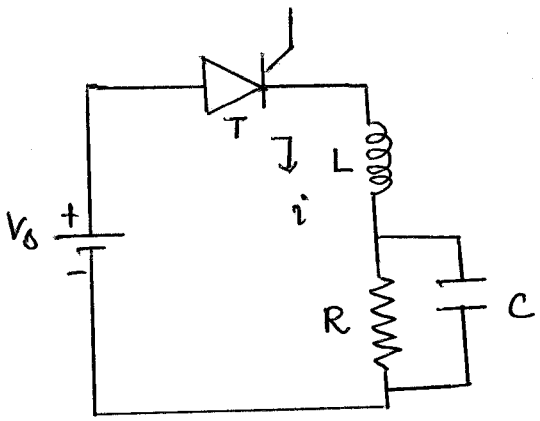
* Here commutation is done by means of commutating components L and C.

* R is load resistance.

* If value of R is less, L and C are connected in series with R.

* If value of R is high, "C" is connected in parallel with R.





* The overall circuit must be underdamped.

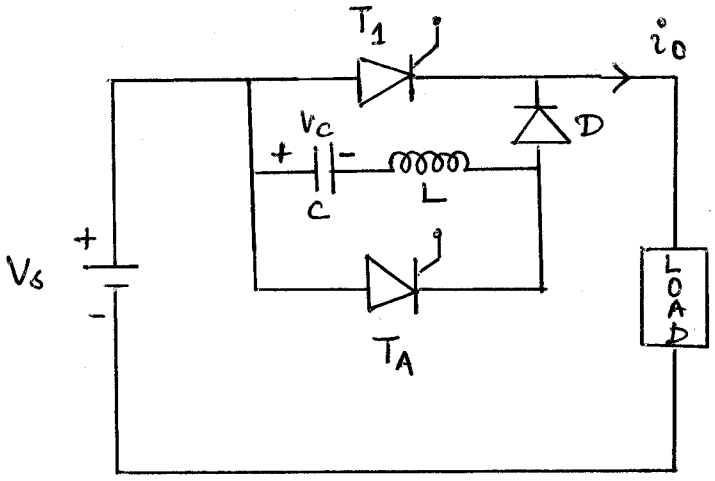
* When current flows through such a circuit having L and C (ie resonant circuit), the current rises to a max value and then decays to zero.

* When the current decays to zero the SCR "T" is turned OFF.

* Class A commutation is possible only in circuits with dc supply.

b) CLASS B (or) RESONANT PULSE COMMUTATION:-

* It is also called as current commutation.



* V_s is source V_{ge}
* T_1 is main thyristor.
* T_A is auxiliary thyristor.
* C is commutating capacitor
* L is commutating inductor.

i_{g1}, i_{gA} = triggering pulse for SCR T_1, SCR T_A.

i_{T_1} = Current through thyristor T_1.

i_c = Capacitor charging current.

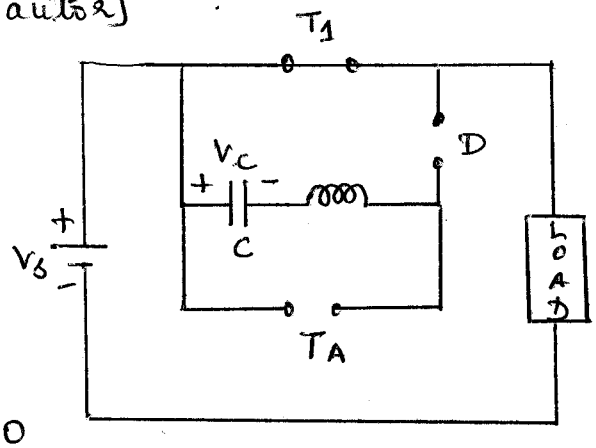
V_c = Voltage across capacitor.

* Capacitor C is fully charged to a values V_s initially with left hand plate +ve; [Precharged capacitor]

Working:

At time $t=0$;

* SCR T_1 is ON
* capacitor is charged to $V_c = V_s$
* ∴ SCR T_1 is ON, V_{ge} across $T_1 = 0$
  i.e., $V_{T_1} = 0$.
* current flows through SCR
  ∴ $i_{T_1} = i_o = I_o$
  I_o = load current.



[* when device is ON its represented by a short circuit and when it is OFF it is represented by open circuit].

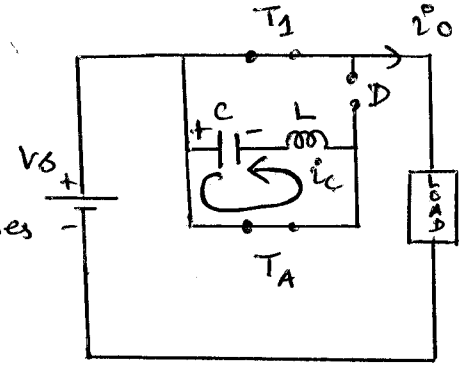
* SCR T_A is OFF
* Diode D is reverse biased so its OFF.

$i_c = 0$ / ∴ there is no path for current to flow.

At $t = t_1$:-

* SCR T_A is turned ON.
* when SCR T_A is turned ON to commutate SCR T_1; Capacitor discharges thro' SCR T_A.
* Capacitor current i_c starts flowing. i_c is in the negative direction $\therefore$ $i_c = -V_s * \sqrt{\frac{C}{L}} \sin \omega_0 t$.
* As $i_c \uparrow$; $V_c \downarrow$. $\because$ the capacitor discharges, V_c decreases.

$\therefore$ $i_o = i_{T_1} = I_o$



After t_1 :-

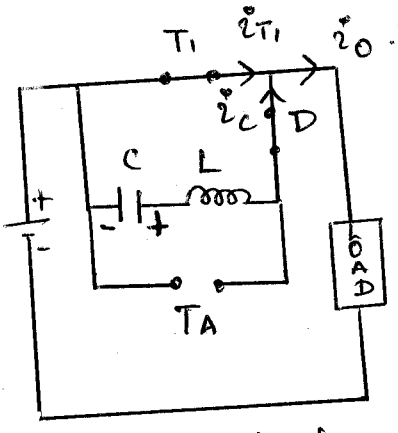
* The negative capacitor current increases and reaches a peak value $i_c = -I_p$
* when i_c reaches peak value (-ve) is at $i_c = -I_p$; the capacitor completely discharges and the Vge across the capacitor $V_c = 0$.
* Now due to the flow of i_c, capacitor starts charging in the reverse direction.
* i_c falls from its -ve peak value I_p to zero.

At $t = t_2$:

* when i_c reaches zero, and capacitor charges in reverse direction to $V_c = -V_s$, SCR T_A is turned OFF (due to reverse Vge and zero ant)
* diode D is forward biased and is turned ON.
* So capacitor discharges through L and D; Now i_c starts flowing in the +ve direction

$\therefore$ $i_o = i_{T_1} + i_c$; (or) $i_{T_1} = i_o - i_c$.

i_c starts $\uparrow$ in +ve direction.



At $t = t_3$; * $v_c = -V_s$.

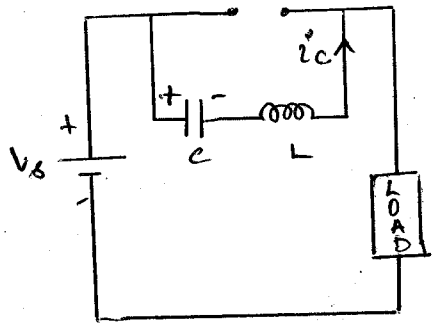
*When i_c ↑es and reaches a i_o ie when $i_c = i_o$, $i_{T_1} = i_o - i_c$

$i_{T_1} = i_o - i_o = 0$;

∴ when current through SCR $T_1 = 0$; SCR T_1 turns OFF.

Capacitor charges in opposite direction

At $t = t_4$:-



* Now capacitor charges in the opposite direction from $-V_s$ to zero.

* At $t = t_4$; $v_c = 0$ and $i_o = i_c$.

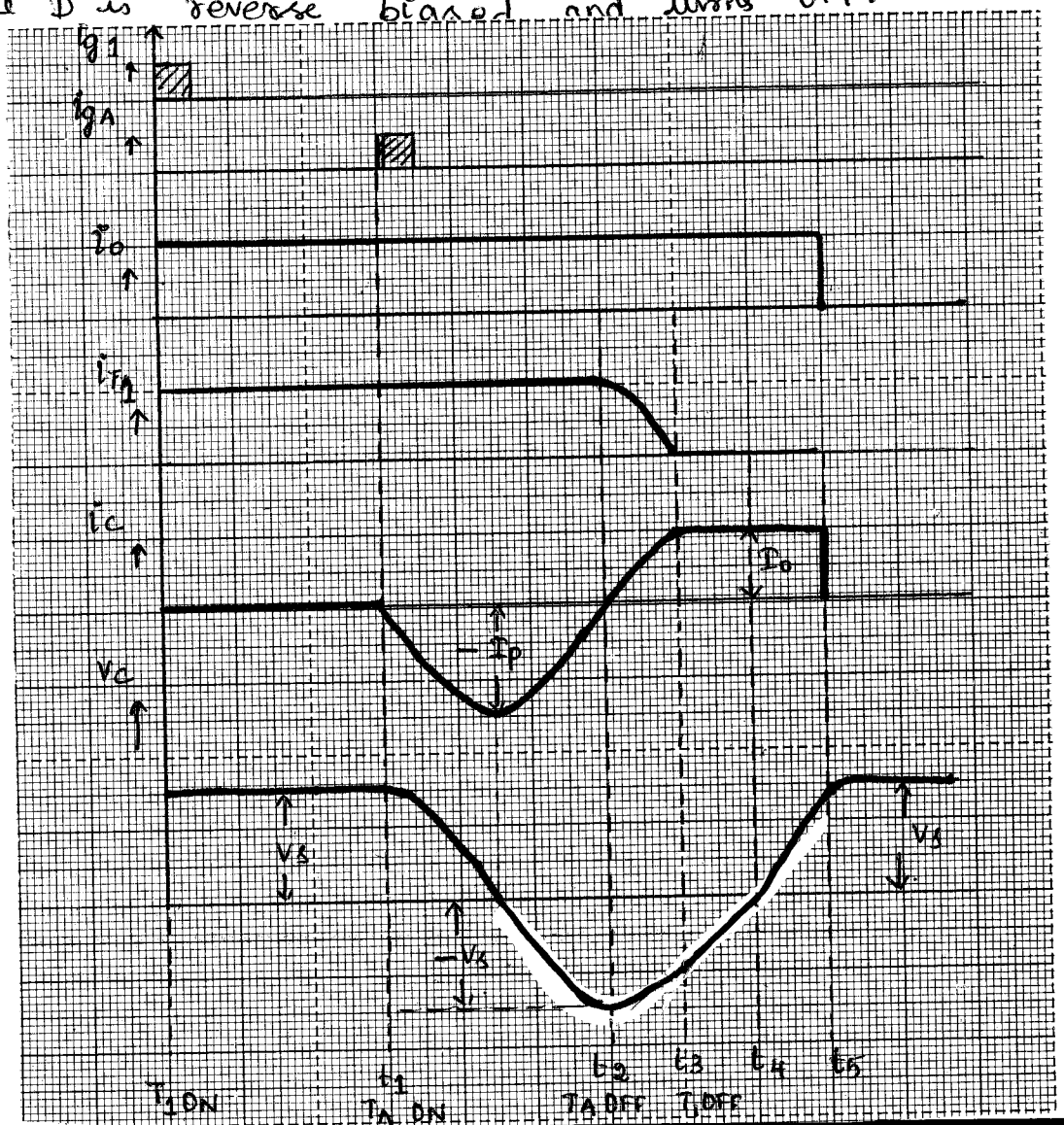
* Capacitor charges from 0 to V_s.

At $t = t_5$:-

i_c ↓ and reaches zero; $i_c = 0$.

$v_c = V_s$.

diode D is reverse biased and turns OFF.

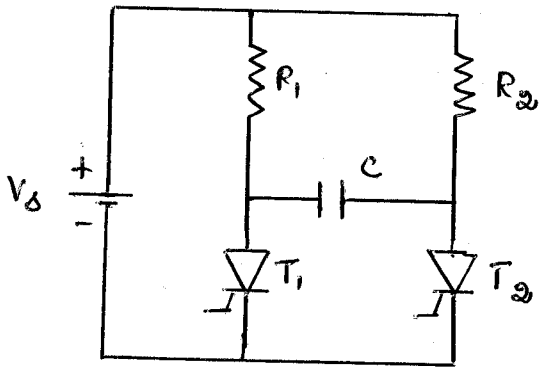


c) CLASS 'C' (or) COMPLEMENTARY COMMUTATION:-

* SCR carrying load current is commutated by transfering its load current to another incoming SCR.

* Here we have two SCRs T_1 and T_2.

Firing T_2; will turn OFF T_1 and Firing T_1 will turn OFF T_2.

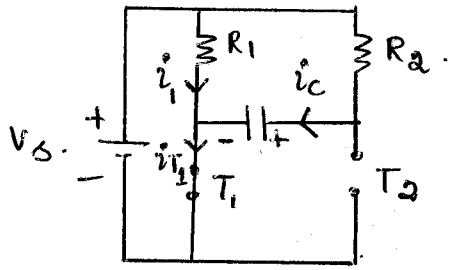


* Capacitor C is initially uncharged.

Mode 1: when SCR T_1 is turned ON at time $t=0$.

* SCR T_1 is ON

  T_2 is OFF.



* V_{gk} across $T_1 = 0$
* current thro' $R_1 = i_1 = \frac{V_s}{R_1}$
* current thro' $R_2 = i_c = \frac{V_s}{R_2}$.
* Thyristor current $i_{T_1} = i_1 + i_c = \frac{V_s}{R_1} + \frac{V_s}{R_2} = V_s\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$.
* Capacitor 'c' starts charging with right hand plate +ve, due to i_c.

$$V_s = i_c R_2 + \frac{1}{C}\int i_c\, dt.$$

$$\frac{V_s}{s} = R_2 I_c(s) + \frac{1}{C}\frac{I_c(s)}{s}$$

$$\frac{V_s}{s} = I_c(s)\left[R_2 + \frac{1}{Cs}\right] = I_c(s)\left[\frac{R_2 Cs + 1}{Cs}\right]$$

$$I_c(s) = \frac{V_s}{s} * \frac{Cs}{R_2 Cs + 1} = V_s * \frac{C}{R_2 Cs + 1}$$

$$\frac{2V_s}{s} = I_c(s)\left[R_1 + \frac{1}{Cs}\right]$$

$$\frac{2V_s}{s} = I_c(s)\left[\frac{R_1Cs+1}{Cs}\right]$$

$$I_c(s) = \frac{2V_s}{s} * \frac{Cs}{R_1Cs+1} = \frac{2V_s * C}{R_1C\left(s+\frac{1}{R_1C}\right)} = \frac{2V_s}{R_1} * \frac{1}{\left(s+\frac{1}{R_1C}\right)}$$

$$\boxed{i_c(t) = -\frac{2V_s}{R_1}e^{-t/R_1C}}$$

-ve sign ∵ current is in reverse direction.

$$V_c(t) = V_s + \frac{1}{C}\int_0^t i_c(t)\,dt = \frac{1}{C}\int_0^t -\frac{2V_s}{R_1}\cdot e^{-t/R_1C}\,dt + V_s$$

$$= -\frac{1}{C} * \frac{2V_s}{R_1} * \left[\frac{e^{-t/R_1C}}{-\frac{1}{R_1C}}\right]_0^t + V_s$$

$$= +\frac{1}{C} * \frac{2V_s}{R_1} * R_1C\left[e^{-t/R_1C} - e^{0}\right] + V_s$$

$$= +2V_s\left[e^{-t/R_1C} - 1\right] + V_s$$

$$= 2V_s \cdot e^{-t/R_1C} - 2V_s + V_s$$

$$= 2V_s \cdot e^{-t/R_1C} - V_s$$

$$\boxed{V_c(t) = V_s\left[2 \cdot e^{-t/R_1C} - 1\right]}$$

* Vge across $T_1 = V_c(t)$.
* when capacitor is charged to $V_c = -V_s$, i_c decays to zero.
* when capacitor is charged to $V_c = -V_s$; $i_c = 0$; $i_{T_2} = i_2 + i_c = i_2 + 0 = i_2$

$\therefore i_{T_2} = i_2 = \frac{2V_s}{R_2}$.

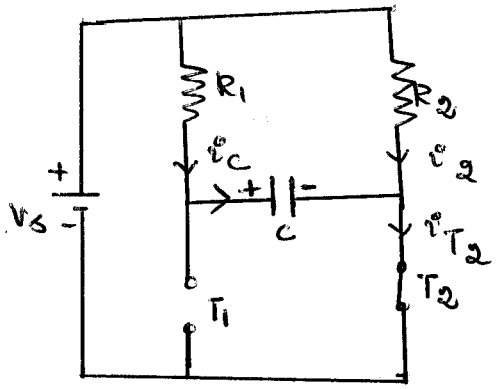
III^{rly} to turns OFF T_2; T_1 is turned ON.

Mode 2:

* When we want to turn OFF T_1 ; T_2 is turned ON.

* Say at $t = t_1$; SCR T_2 is turned ON.

* When T_2 is ON, the capacitor Vge V_c applies a reverse Vge across T_1 and turns T_1 OFF. (or) [Capacitor discharges through T_2 ; reverse current flows thro' T_1 so T_1 is OFF).



* Vge across $T_2 = 0$, i.e., $V_{T_2} = 0$

* current thro' $R_2 = i_2 = \frac{V_s}{R_2}$

* current thro' $R_1 = i_c = -\frac{2V_s}{R_1}$

(-ve sign because cunt flows in opposite direction)

$$\therefore \quad i_{T_2} = i_2 + i_c = \frac{V_s}{R_2} + \frac{2V_s}{R_1} = V_s\left(\frac{2}{R_1} + \frac{1}{R_2}\right)$$

$$i_{T_2} = V_s\left[\frac{2}{R_1} + \frac{1}{R_2}\right]$$

Due to current i_c flowing, capacitor starts charging from $+V_s$ to $-V_s$ with left hand plate +ve.

$$V_s = R_1 i_c + \frac{1}{C}\int i_c \, dt$$

$$\frac{V_s}{s} = R_1 I_c(s) + \frac{1}{C}\left[\frac{I_c(s)}{s} + \frac{q(0)}{s}\right]$$

$$\left[q(0) = C.V_c(0) \quad q(0) = -CV_s\right]$$

$$\frac{V_s}{s} = R_1 I_c(s) + \frac{1}{C}\left[\frac{I_c(s)}{s} - \frac{CV_s}{s}\right]$$

$$\therefore \quad \frac{V_s}{s} = R_1 I_c(s) + \frac{1}{C}\cdot\frac{I_c(s)}{s} - \frac{1}{\cancel{C}} * \frac{\cancel{2}V_s}{s}$$

$$\frac{V_s}{s} = R_1 I_c(s) + \frac{1}{C}\frac{I_c(s)}{s} - \frac{V_s}{s}$$

$$I_C(s) = V_s * \frac{C}{R_2 C s + 1} = \frac{V_s * \frac{1}{R_2 C}}{R_2 \frac{1}{R_2 C}\left(s + \frac{1}{R_2 C}\right)} = \frac{V_s}{R_2} * \frac{1}{\left(s + \frac{1}{R_2 C}\right)}$$

taking inverse laplace.

$$\boxed{i_C(t) = \frac{V_s}{R_2} \cdot e^{-t/R_2 C}}$$ = current thro' capacitor.

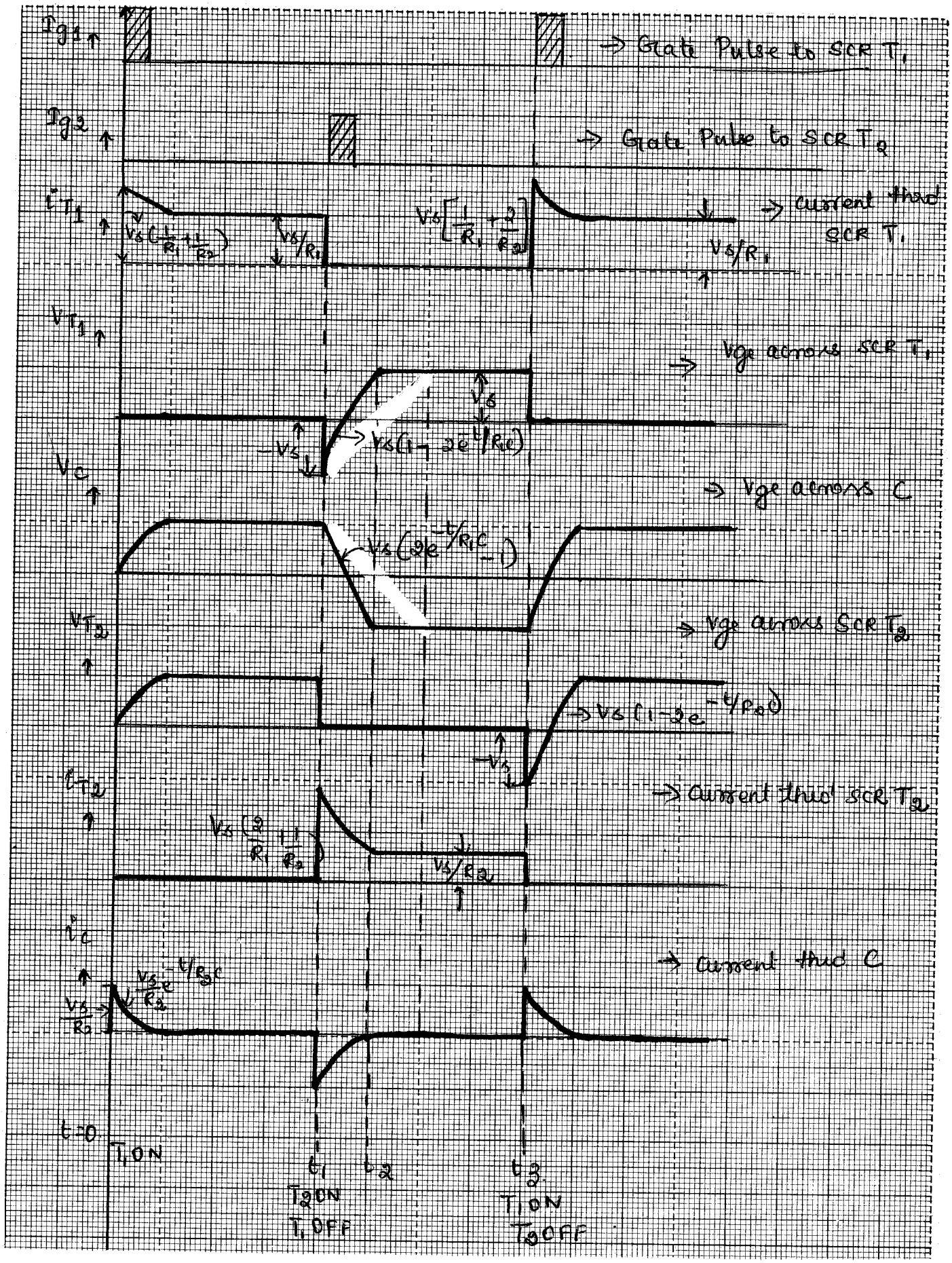
$$\therefore V_C(t) = \text{Vge across capacitor} = \frac{1}{C}\int_0^t i_C(t)\,dt = \frac{1}{C}\int_0^t \frac{V_s}{R_2} \cdot e^{-t/R_2 C}\,dt$$

$$\therefore V_C(t) = \frac{1}{C}\cdot\frac{V_s}{R_2}\left[\frac{e^{-t/R_2 C}}{\frac{-1}{R_2 C}}\right]_0^t = \frac{1}{C} * \frac{V_s}{R_2} * -R_2 C\left[e^{-t/R_2 C}\right]_0^t$$

$$= -V_s\left[e^{-t/R_2 C} - e^{0}\right] = -V_s\left[e^{-t/R_2 C} - 1\right] = V_s\left[1 - e^{-t/R_2 C}\right]$$

$$\therefore \boxed{V_C(t) = V_s\left[1 - e^{-t/R_2 C}\right]}$$

* Vge across $T_2 = V_C(t)$
* when capacitor is fully charged to $V_C = V_s$; the capacitor current i_C decays to zero.
* At $V_C = V_s$; $i_C = 0$; $\therefore i_{T_1} = i_1 + i_C = i_{T_1} = i_1 + 0 = \frac{V_s}{R_1}$
* $i_{T_1} = i_1 = \frac{V_s}{R_1}$


T_{g1}
T_{g2}
i_{T_1}
V_{T_1}
V_C
V_{T_2}
i_{T_2}
i_C
$V_s\left(\frac{1}{R_1}+\frac{1}{R_2}\right)$
V_s/R_1
$V_s\left[\frac{1}{R_1}+\frac{2}{R_2}\right]$
V_s/R_1
$-V_s$
$V_s(1-2e^{-t/R_1C})$
$V_s(2e^{-t/R_1C}-1)$
$-V_s$
$V_s(1-2e^{-t/R_2C})$
$V_s\left(\frac{2}{R_1}+\frac{1}{R_2}\right)$
V_s/R_2
$\frac{V_s}{R_2}e^{-t/R_2C}$
$\frac{V_s}{R_2}$
$t=0$
T_1 ON
t_1
T_2 ON
T_1 OFF
t_2
t_3
T_1 ON
T_2 OFF
→ Gate Pulse to SCR T_1
→ Gate Pulse to SCR T_2
→ current thro' SCR T_1
→ Vge across SCR T_1
→ Vge across C
→ Vge across SCR T_2
→ current thro' SCR T_2
→ current thro' C

d) CLASS D COMMUTATION / AUXILIARY OR IMPULSE COMMUTATION:-

* It is also called as voltage commutation.

* T_1 is the main SCR.

* T_A is the auxiliary SCR

* Capacitor C is precharged with upper plate positive.

$\therefore V_C = +V_s$

* load current i_o is constant ie, $i_o = I_o$.

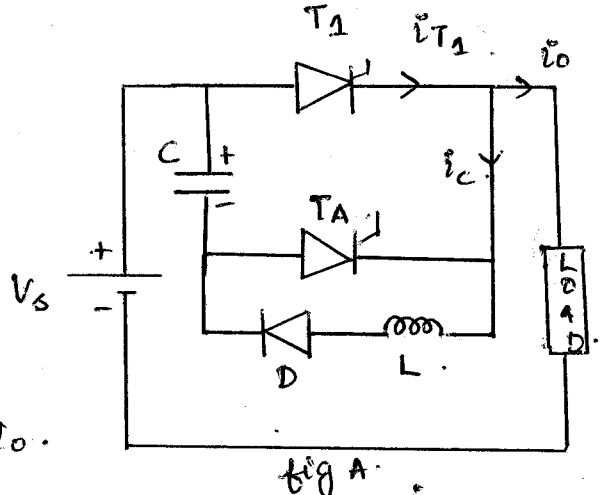


fig A

At time t=0:-

* SCR T_1 is ON ; T_A is OFF.

* Vge across T_1 = $V_{T_1} = 0$

* Current thro' T_1 = $i_{T_1} = \uparrow$

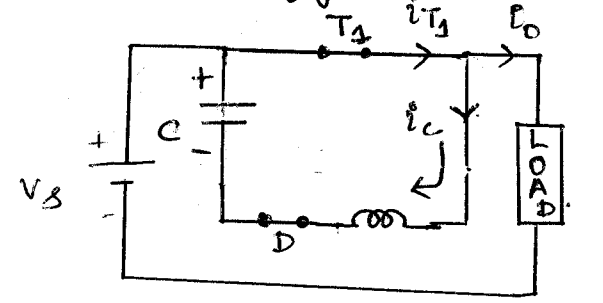


fig B

* Vge across the capacitor forward biases the diode. Diode conducts

* So a circuit is formed between C – T_1 – L – D – C. Current i_c flows thro' this circuit

* $\therefore$ Capacitor discharges through diode.

$\therefore$ $V_c = V_s$ starts ↓ing. [$V_c \downarrow$; $i_c \uparrow$]

i_c ↑es.

$\therefore$ $i_{T_1} = i_c + i_o$. [from fig B]

After some time: [Some time after t=0]

* when i_c reaches maximum value, the capacitor Vge is completely discharged and is equal to zero.

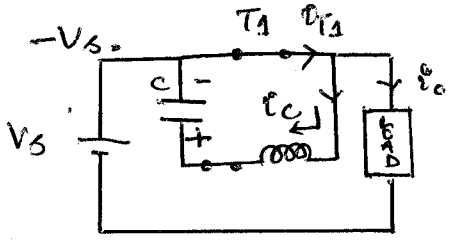
& at $i_c = i_{c\,max}$; $V_c = 0$.

$\therefore$ $i_{T_1} = i_{c\,max} + i_o$

* After reaching the maximum value the capacitor current starts decreasing. So the capacitor will be charged in

the reverse direction with lower plate positive towards $-V_s$.

$\therefore$ as $i_C \downarrow$; $V_C \uparrow$ i.e $V_C \uparrow$ towards $-V_s$.



* At some time when i_C is completely equal to zero the capacitor would have been fully charged on the -ve direction. So diode D is reverse biased and is turned OFF.

i.e at $i_C = 0$; $V_C = -V_s$.

At this instant $\therefore$ $i_{T_1} = i_C + i_o = 0 + i_o$

$\therefore$ $i_{T_1} = i_o$.

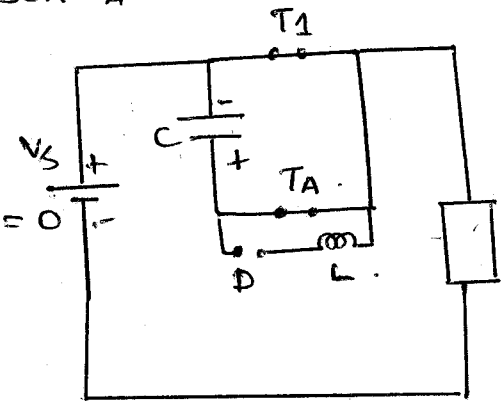
At $t = t_2$:-

* when we want to turn OFF SCR 1 ; SCR T_A is turned ON.

$\therefore$ at $t = t_2$.

* T_1 is ON ; * T_A is turned ON.

* diode D is OFF ; $V_C = -V_s$; $i_C = 0$



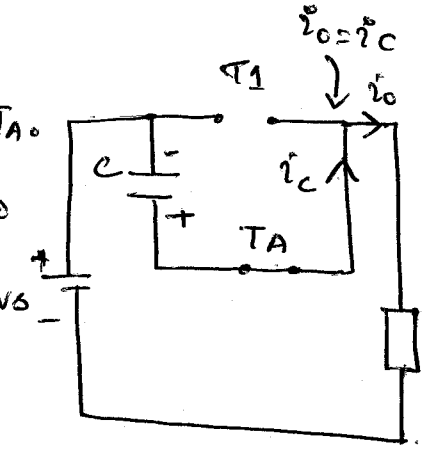
* Now since SCR T_A is ON, the capacitor Vge $V_C = -V_s$, reverse biases SCR T_1 and turns it OFF.

* So now the capacitor C discharges thro' SCR T_A.

* So i_C flows in reverse direction and V_C also charges on reverse direction.

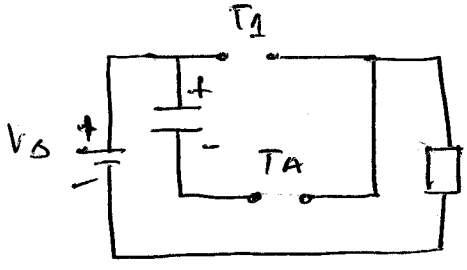
$\therefore$ i_C flows in opposite direction.

$V_C \uparrow$ charges towards $+V_s$



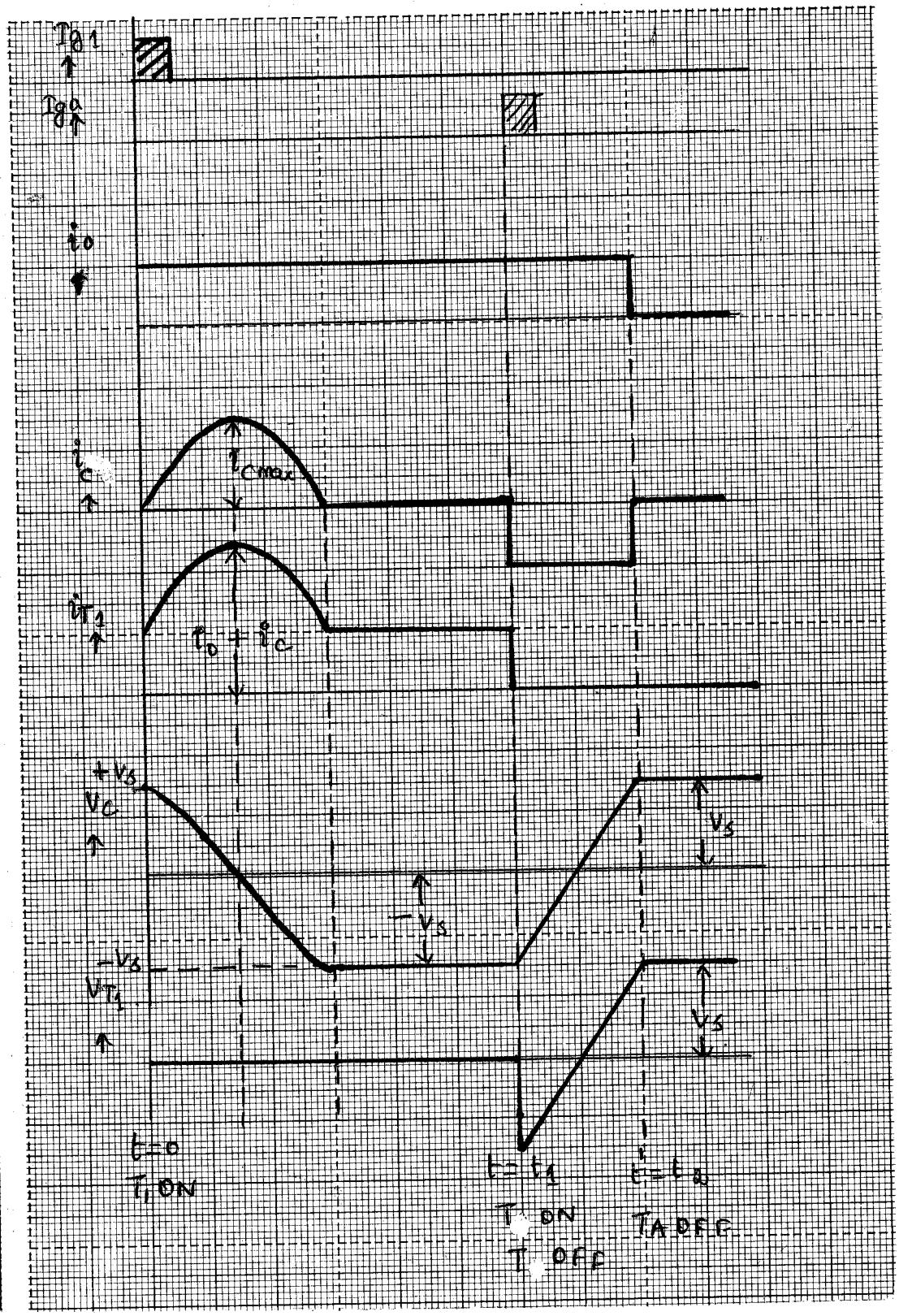
$\therefore$ SCR T_1 is OFF ; $i_{T_1} = 0$

$\therefore$ $i_o = i_C$.

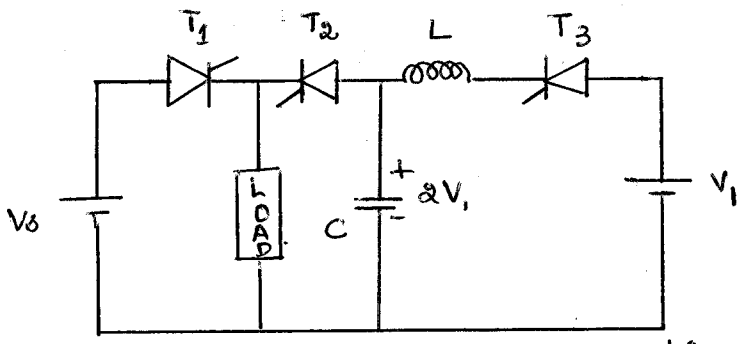


At $t = t_3$;- when $V_C \uparrow$ and reaches $V_C = V_s$, $i_C = 0$

at this time current thro' T_A is 0 and is turned OFF at $t = t_3$.


T_{g1}
T_{g2}
i_0
i_C
I_{CMax}
i_{T_1}
$I_0 + i_C$
$+V_S$
V_C
$-V_S$
V_{T_1}
V_S
$-V_S$
V_S
$t=0$
T_1 ON
$t=t_1$
T_1 ON
T_1 OFF
$t=t_2$
T_A OFF

e) CLASS E COMMUTATION [OR] EXTERNAL PULSE COMMUTATION:



* T_1 is main SCR
* T_2, T_3 commutating SCR.
* V_s is main source.
* V_1 is auxiliary supply.

* In this type of commutation an external pulse from a seperate voltage source(V_1) is used to turn OFF SCR T_1,

* Initially * SCR T_1 is ON
* load is connected across V_s.

* when T_3 is turned ON, the capacitor C charges to $V_C = +2V_1$ through $V_1 - T_3 - L - C - V_1$. (oscillator circuit)

* Since current through capacitor = i_c is oscillatory it falls to zero. when i_c falls to zero T_3 is turned OFF.

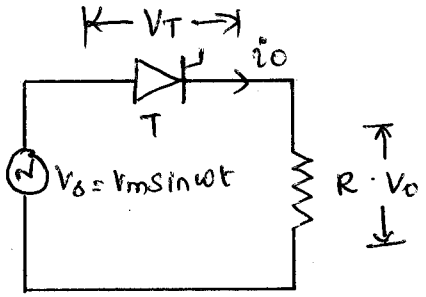
* To commutate T_1, T_2 is turned ON.

* when T_2 is ON the voltage across the thyristor T_1 is reverse biased.

i.e., T_1 is subjected to a reverse voltage equal to $V_s - 2V_1$.

∴ SCR T_1 is turned OFF. and capacitor discharges through the load.

f) CLASS F COMMUTATION [OR] LINE COMMUTATION:-



* This is also called as natural commutation.
* V_s is ac $V_{gen} = V_s = V_m \sin\omega t$.
* Say at time $\omega t = 0$ SCR T is ON.

$\therefore V_T = 0$; $i_T \uparrow$.

* At time $\omega t = \pi$; $V_s = 0$ i.e supply voltage is zero and is negative after that.
* At this instance SCR T is reverse biased and is turned OFF.