SE | IT | III (REV) 29|5|2012
Digital logic Design & Application

Con. 4469 GN-8348

(3 Hours) [Total Marks 100

N.B.N. B. : (1) Question NO.1 is compulsory. .
(2) Solve any four out of remaining six questions.

1. a. Convert $(243)_5$ into equivalent base 8 number and base 7 number. (4)

b. Perform the following operations – (6)

1) $(F8F)_{16} + (D49)_{16}$
2) $(762)_{BCD} + (238)_{BCD}$
3) $(246)_{10} - (435)_{10}$ using 2's complement method.

c. Convert SR flip flop to JK flipflop. (5)

d. With the help of suitable example, explain how hamming code is able to locate and correct single bit error. (5)

2. a. Implement one digit BCD adder using IC 7483. Explain its working. Expand your design to implement 4 digit BCD adder. (10)

b. Implement 2 bit comparator using active low decoder. (10)

3. a. Implement 4 bit Asynchronous up counter. Also sketch the timing diagrams. (10)

b. Explain bidirectional shift register with the help of neat diagram. (10)

4. a. Design Mod 12 synchronous up counter using JK Flipflops and NAND gates only. Design the counter as lock out free counter. (12)

b. Script VHDL Code for 3 :8 decoder (8)

5. a. Draw the circuit diagram of TTL NAND Gate and explain its working. (10)

b. Implement full adder using two 4:1 Multiplexers and additional gates (10)

6. a Using Quine McClusky method of minimization minimize (10)
$F = \Sigma m (8,9,10,11,13,15,16,18,21,24,25,26,27,30,31)$.

.b Implement BCD to Excess 3 code converter using NOR Gates only. (10)

7. Write short notes on any two. (20)
a. CAD Tools
b. Race around condition and its remedy in master slave JK Flip flop.
c. Programmable logic devices
d. Priority encoders.