*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/B.TECH (CSE/IT/PWE/EEE)/SEM-5/EI-502/2011-12**

# 2011

# MICROPROCESSOR & MICROCONTROLLER

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A

## ( Multiple Choice Type Questions )

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) In 8085 the addressable memory is

a) 64 kB b) 1 MB

c) 4 KB d) 16 KB.

ii) The addressing mode of the instruction LDA address is

a) Combined b) Implied

c) Register d) Direct.

iii) The instruction XCHG exchanges the contents of

a) ACC and HL pair

b) BC pair and HL pair

c) DE pair and HL pair

d) HL pair and memory location.

iv) Machine cycles for 1 N instruction are

a) 6 b) 5

c) 4 d) 3.

v) The content of the Accumulator is 08 H, then the XRI 80 H instruction was executed. The content of the accumulator is

a) 80 H b) FF H

c) 88 H d) 08 H

vi) RST 7·5 interrupt is

a) Vectored and Maskable

b) Non-vectored and Maskable

c) Non-vectored and Non-maskable

d) Vectored and Non-maskable.

vii) When a subroutine is called the address of the instruction next to CALL is saved in

a) Stack pointer

b) Program Counter

c) Stock

d) Combinatio of flag and AX register.

viii) An 8 K ∞ 8 ROM, holding the monitor program in a microprocessor trainer kit has the end address

a) 8000 H b) 4000 H

c) 1 FFF H d) 3 FFF H.

ix) How many address lines are there in 8086 microprocess ?

a) 16 b) 8

c) 20 d) 12.

x) The total I/O space available in 8085 if used peripheral mapped I/O.

a) 64 b) 128

c) 256 d) 512.

xi) 8251 is a

a) USART IC b) Counter

c) interrupt controller d) none of these.

xii) A single instruction to clear the lower four bits of the accumulator in 8085 microprocessor is

a) XRI OF H b) ANI FOH

c) ANI OF H d) XRI FOH.

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following. 3 × 5 = 15

2. State the uses of any three special purpose registers available in 8085 microprocessor.

3. Draw the timing waveform of op-code fetch machine cycle of 8085 microprocessor.

4. Write a subroutine for 1 sec delay using 8085 assembly level instructions.

5. a) What are the functions of ALE, HOLD and READY signals ? 3

b) Define machine cycle and instruction cycle. 2

6. a) Give the bit configuration of 8085 flag register. 2

b) Write down the mode-0 control word of 8255 A for the following : 3

PORT *A* = input, PORT *B* not used,

PORT *C* ( upper ) = input, PORT *C* ( lower ) = output.

## GROUP – C

### ( Long Answer Type Questions )

Answer any *three* of the following. 3 × 15 = 45

7. a) What are different interrupts in 8085 ? Give their locations. Distinguish between maskable and unmaskable interrupts. 2 + 2 + 2

   b) After the execution of RIM instruction, the accumulator contains 49 H. Explain the accumulator contents. 5

   c) Which interrupts are marked after the execution of the following instructions ?

   MVI A, 1 DH, SIM. 4

8. a) Discuss the advantages and disadvantages of memory mapped I/O and I/O mapped I/O scheme. Which scheme is supported by the 8085 microprocessor and how ? 3 + 2

   b) Give the hardware and software to interface, one seven-segment display with 8085 $\mu$p whose address is FC 23 H. 6

   c) Which addressing mode is used in the above scheme ? What change is required if address of the display is FCH ? 4

9. a) Describe the different addressiing modes of 8086 microprocessor. 6

   b) What are the main functions performed by BIU and EU unit of 8086 microprocessor ? 5

   c) How is pipeline achieved in 8086 microprocessor ? 4

10. Discuss the hardware and software of any microprocessor-based industrial application.

11. Write notes on any *three* of the following : 3 × 5

    a) Synchronous mode of data transfer

    b) Interrupt Service Subroutine

    c) BSR mode of 8255 PPI

    d) Designing I/O ports

    e) Serial mode of operation using 8085 microprocessor.