Max. Marks: 100

Reg.	No.:	********	*********	******
Name				

VI Semester B.Tech. Degree (Reg./Supple./Imp. – Including Part Time) Examination, May 2014

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(2007 Admn. Onwards)

PT 2K6/2K6EC 606 (F): ANALOG MOS CIRCUITS

Time: 3 Hours

Instructions: 1) Answer all questions in Part - A.

2) Answer one question from each Module in Part - B.

PART-A

	PARI – A		
1.	a) Explain the physical structure of n-channel enhancement type MOSFET		5
	b) Describe MOS resistors and resistor circuits.		5
	c) Define MOS current steering circuits.		5
	d) Define Coscoding.		5
	e) Explain the basic gain cell in IC amplifier. Define intrinsic gain.		5
	f) Explain CMRR.		5
	g) Explain level shifting in multiplexes.		5
	h) Write short note on clocked comparators.		5
		$(8 \times 5 =$	40)
		P.	T.O.

PART-B

	a)	Explain the formation of a channel for current flow in n-channel MOSFET. OR	15
	b)	Consider a process technology for which $L_{min} = 0.4$ ym, $t_{ox} = 8$ nm, $Y_n = 450$ cm ² /V.s and $V_t = 0.7$ V.	
		a) Find C _{ox} and process conductance parameter (K _n ¹).	
		 b) For a MOSFET with W/L = 8 ym calculate the values of V_{GS} and V_{DSmin} needed to operate the transducer in saturation region with a DC current I_D = 100 μA. c) For the device in (b) find the valve of V_{GS} required to course the device to operate as a 1000 Ω resistor for very small V_{DS}. 	15
111.	a)	parameters R _{in} A _{VO} and R _O .	15
	b)	Describe Wilson MOS mirror.	15
IV.	a)	Describe current-source loaded common source Amplifier. OR	15
	b)	Describe small signal analysis of common Gut Amplifier with active loads.	15
٧.	a)	Explain switched capacitor implementation of ladder filter. OR	15
	b)	Explain CMOS comparator design. (4×15=6	15