Roll No. | | | | | | | | | | |

B.E / B.Tech (PartTime) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014

ELECTRONICS AND COMMUNICATION ENGINEERING

Semester II

PTEC8201Digital Electronics and System design

(R 2013)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Convert 101.101 to binary number system
2. Express the Boolean function F=A'+BC as sum of minterms.
3. Realize Full adder using two half adders.
4. Compare PLA with PAL.
5. State the difference between Moore and Mealy state machines.
6. Draw the Truth table and Excitation table of JK Flip Flop.
7. What is meant by stable state in asynchronous sequential circuits?
8. Illustrate the advantages of Asynchronous sequential circuits over synchronous sequential circuits.
9. Draw the logic circuit of a basic RAM cell.
10. State the differences between SRAM and DRAM.

Part – B (5 x 16 = 80 marks)

11. i) Obtain the reduced primitive flow table in the design of a latch circuit with two inputs D and G and an output Q. Output Q will be equal to input D when G=1 and retains this value after G goes to 0.Once G=0, a change in D does not change the value of the output Q. (10)

    ii) Describe the hazards in the combinational and sequential logic circuits. (6)

12. a) i) Simplify the Boolean function using K Map.
    $Y(A,B,C,D,E)=\sum(1,2,5,6,7,10,12,13,14,28,29,30,31)$
    Don't care conditions $d(8,17,18,24,27)$ (10)

    ii) Realize the resulting simplified function from Q.12.a.(i) using only NAND gate. (6)

    (OR)

    b) i)Simplify the Boolean function using Tabular minimization method.
    $F(A,B,C,D,E)=\sum(0,2,4,5,6,7,8,10,14,17,18,21,29,31)$ (12)

ii) Design a binary to octal code converter. (4)

13. a) i) What is an encoder circuit and discuss the problem associated with it. (4)

ii) Design a 4 bit priority encoder and implement it using AND -OR logic gates. Consider the inputs with the increasing priority from D_0,D_1,D_2 and D_3. (12)

(OR)

b) i) Design a 4 bit binary parallel adder. Discuss the drawback associated with it and then design a circuit which can overcome the drawback.

14. a) i) Design a Clocked sequential Counter circuit whose output goes from 0,2,4,6,8,10,12,14,0....Use T flip flops for the design. (16)

(OR)

b) i) Reduce the following state table and draw the reduced state diagram. (8)

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

ii) Draw the logic circuit of switch tail ring counter. What is the significant advantage of it over ring counter? (8)

15. a) i)Draw and explain the 2 input NAND gate in open collector and Totem pole TTL logic family. (12)

ii) Compare the Noise margin, Fan out and Propagation delay characteristics of TTL logic family gates with that of CMOS logic family.

(OR)

b) i) Draw and explain the 2 input NAND and NOR gate circuits in CMOS logic family. (10)

ii) Explain the Address multiplexing scheme for 64K DRAM. (6)