9/12/09

Lab

40 : 2ndExm.09-AM(a)

ME / ETRX / sem II

micro - and System II

10:30 to 12:30

Con. 5119-09.

BB-6158

Microprocessors & System II

(3 Hours) [Total Marks : 100

(14)

N.B.: (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** questions out of **remaining** questions.
(3) State any additional **data** assumed, if **necessary** to answer.

1. (a) With suitable diagrams explain superscalar nature and pipe line features for Pentium. **10**
   (b) Giving timing diagram, explain when and how the burst bus cycles are conducted by Pentium. **10**

2. (a) Explain reflected wave switching and its use in PCI bus. Why bus parking is needed ? How it is done ? **10**
   (b) Explain how interrupts are handled in PCI bus. **10**

3. (a) Describe the data and code cache structures in detail for Pentium. **10**
   (b) Explain cache control signals of Pentium. How they can be used to maintain cache coherency in the Pentium based machine ? **10**

4. (a) Explain with suitable diagrams how data transactions occur on the USB bus. **10**
   (b) Explain how bus arbitration is achieved in PCI bus. What is hidden bus arbitration ? **10**

5. (a) Describe the requirements for a real time operating system. **10**
   (b) Explain the functions of microkernel for QNX operating system. **10**

6. (a) Explain the functions of following PCI signals. **10**
   (i) $\overline{\text{FRAME}}$ (ii) $\overline{\text{IRDY}}$ (iii) $\overline{\text{DEVSEL}}$ (iv) SDONE (v) $\overline{\text{SBO}}$
   (b) Explain bus access Latency for PCI bus. Explain the function of Latency Timer. **10**

7. Write notes on any **two** of the following :— **20**
   (a) Fire Wire bus
   (b) Special bus cycles for Pentium
   (c) Branch prediction logic of Pentium
   (d) System management mode in Pentium.