*Name* : .....

*Roll No.* : .....

*Invigilator's Signature :* .....

**CS/B.TECH/ECE(OLD)/SEM-4/EC-402/2013**

# 2013

# DIGITAL ELECTRONIC CIRCUITS

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A

## ( Multiple Choice Type Questions )

1. Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i) Gray code is called

a) reflected code b) non-weighted code

c) unit distance code d) all of these.

ii) The number of select lines in a 16 : 1 multiplexer is

a) 4 b) 3

c) 2 d) 1.

iii) $(1AF)_{16}$ =

a) $(567)_8$ b) $(576)_8$

c) $(657)_8$ d) $(557)_8$.

iv) The complement of exclusive OR function is

a) $AB + A'B$ b) $AB + A'B'$

c) $A'B + A$ d) $AB + AB'$.

v) $A + B'C$ =

a) $\sum m(0,2,3)$ b) $\Pi M(1,4,5,6,7)$

c) $\sum m(1,4,5,6,7)$ d) $\Pi M(1,2,5,6,7)$.

vi) A 4 bit ripple counter uses flip-flop with propagation delay of 50 ns each. The maximum clock frequency which can be used is

a) 5 MHz b) 10 MHz

c) 20 MHz d) 25 MHz.

vii) In a sequential circuit the output at any instant depends on

a) present inputs only

b) past inputs only

c) past outputs only

d) present input and past output.

viii) A 10 bit D/A converter gives a maximum output of 10·23 V. The resolution is

a) 10 mV b) 20 mV

c) 15 mV d) 25 mV.

ix) TTL stands for

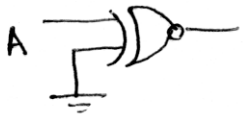
a) Transistor Transistor Logic

b) Transistor Transformer Logic

c) Transistor Transfer Logic

d) none of these.

x) For the gate given below the output will be




a) 0 b) 1

c) $A$ d) $A'$.

xi) In JK flip-flop, the input $J = K = 1$ pulse is as out

a) set b) reset

c) no change d) toggle.

xii) Which one of the following can be used as parallel to series converter ?

a) Decoder b) Digital counter

c) Multiplexer d) Demultiplexer.

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following. $3 \times 5 = 15$

2. Design a full adder circuit using two half adder circuits (with truth table).

3. Design a 16 : 1 MUX using 4 : 1 MUX.

4. Design a two-bit comparator circuit by using minimum number of gates.

5. Draw and explain successive approximation type A/D converter.

6. What is race around condition ? How can you eliminate this problem ? Explain with proper diagram. 1 + 4

## GROUP – C
## ( Long Answer Type Questions )

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Design the following circuits using universal gates ( NAND and NOR ) :

   i) AND

   ii) OR

   iii) X-OR.

   b) Simplify the following using *K*-map :

   i) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$

   ii) $F(A,B,C,D) = \Pi M(1,2,3,8,9,10,11,14).d(7,15)$

   c) Distinguish between the combinational circuit and sequential circuits. 3 + 10 + 2

8. a) Design the following using suitable MUX :

   $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

b) Minimize the following function by using Quine McCluskey method :

$$F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$$

c) Design a full adder circuit using decoder and necessary gates. 4 + 8 + 3

9. a) Make the FF conversions :

i) *JK* to *T*

ii) *D* to *SR*.

b) Design a MOD-6 up counter using *JK* flip-flops.

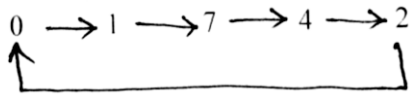
( 2 × 3 ) + 9

10. a) Implement the following two Boolean functions with a PLA :

$$F_1 = \sum m(0,1,2,4)$$

$$F_2 = \sum m(0,5,6,7)$$

b) Design the sequence generator using *T* flip-flops.



11. a) Define the following terms :

i) Propagation delay

ii) Threshold voltage

iii) Fan in

iv) Fan out

v) Speed of response.

b) Design and explain the operation of totem-pole output.

c) Design the universal gates using CMOS only. 5 + 5 + 5

12. Write short notes on any *three* of the following : 3 × 5

a) Priority Encoder

b) Successive Approximation type ADC

c) Parity generator and checker

d) Universal Shift Register

e) BCD to 7-segment display.

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