M.E. Sem I (Rev.) Etrx Microprocessor & System 08/12/08

VT Oct. 08-183

Con. 5214–08. **(REVISED COURSE)** **BB–8207**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume any **suitable data,** wherever **necessary**.

1. Design SBC with following specifications :– **20**
   (a) 80386 DX operates at 25 MHz.
   (b) Firmware support of 256KB using 64KB EPROM devices.
   (c) Data memory support of 2GB using 1GB SRAM devices.
   Draw memory map and show the decoding logic used.

2. Explain the address translation mechanism used in 80386 DX with neat diagrams. **20**
   Support your answer with (i) segment translation (ii) page translation.

3. Explain protection mechanism supported in 80386 DX for code, data and stack **20**
   segments in detail. Support your answer with diagrams.

4. Explain what is TSS. Explain, with neat diagram, task switching mechanism **20**
   of 80386 DX (only Direct Switch).

5. (a) Draw the interfacing diagram which involves 80386 DX and 82385 DX. Explain **10**
   briefly.
   (b) Design 2-way set associative as well as Direct mapped cache organisation **10**
   for the following :–

Main Memory	=	4GB
Cache Memory	=	32KB
Cache Controller	=	82385 DX
Line Size	=	32 bits
One Set	=	8 lines

   Give the directory entry for both in detail.

6. (a) Describe ISA bus cycle for 8-bit memory with timing diagram. **10**
   (b) How ISA bus system can handle 32-bit memory operations. **10**

7. Write short notes :– **20**
   (a) I/O protection mechanism of 80386 DX
   (b) ISA interrupt subsystem.

****