Code No. 5235 / O / S

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I-Semester **(Old)** Examination, June / July 2012

Subject : **Computer Organization Architecture**

Time : 3 Hours Max. Marks: 75

Note: Answer **all** questions of Part - A and answer any **five** questions from Part-B.

PART – A (25 Marks)

1. Show that hardware, including logic gates for the function, that implements the statements : (3)
   $xy'T_0 + T_1 + x'yT_2 : A \leftarrow A + 1$

2. Give the infix notation of the following reverse polish notation : (2)
   AB * CD * + EF * +

3. A compute system has 16-registers, an ALu with 32-Operations and a shifter with eight operations, ill connected to a common bus, formulate a control word for a micro operation. (3)

4. Mention the need for I/O interface module. What are the various functions of these modules? (2)

5. What is the need for IEEE floating point standard? Show the single and double precision floating point notation. (3)

6. Mention the influence of pipelining on Instruction Set design. (2)

7. Show the structure of an Array multiplier. Mention how it is different. (2)

8. A terminal in transmitting Asynchronous Serial data at 2400 bd. What is the bit time? Assuming 7-data bits, parity and a stop bit. How long does it take to transmit one character? (3)

9. Distinguish between synchronous and asynchronous methods of data transfer. (2)

10. Briefly explain the functioning of magnetic disks. (3)

PART – B (5x10=50 Marks)

11. Draw the logic diagram of a 4-bit register with clocked JK flipflops having control inputs for the increment, complement and parallel transfer micro-operations. Show how the 2's complement can be implemented in this register. (10)

12. It is necessary to design a digital circuit with four inputs 'C', 'S','Z' and 'V' and 10 outputs, one for each of the branch conditions.

Relation		Condition of status bits(case(i))	Condition of status bits (case (ii))
(i)	$A > B$	C or Z = 0	Z or $(S \oplus V)=0$
(ii)	$A \geq B$	C = O	$S \oplus V = 0$
(iii)	$A < B$	C = 1	$(S \oplus V) = 1$
(iv)	$A \leq B$	C or Z = 1	Z or . $S \oplus V = 0$
(v)	$A = B$	Z = 1	Z = 1
(vi)	$A \neq B$	Z = 0	Z = 0

Draw the circuit using OR gates, XOR and inventive. (10)

13. Write the programs to evaluate the arithmetic statement
X = (A+B*C) / (D – E * F. + G * H) using
(i) General register type computer with two address instruction.
(ii) Using Accumulator type computer with one-address instruction.
(iii) Using Stack organized computer with zero-address instruction. (10)

14.(a) Demonstrate the performance considerations of pipelining through suitable parameters. (5)
(b) Explain the floating point addition algorithm using suitable flow chart. (5)

15.(a) Explain briefly about various methods of I/O data transfer used in computer system. Comment on their relative merits and demerits with respect to performance. (7)
(b) What are the functions of I/O processor? (3)

16.(a) A computer has a primary and secondary cache. The cache blocks consists of 8 words. Assume that the hit rate is the same for both caches, and that is equal to 0.95 for instructions and 0.9 for data. Assume that the times needed to access an 8-word block in these caches are C_1 = 1 cycle and C_2 = 10 cycles.
(i) What is the average access time experienced by the CPU of the main memory uses interleaving? And what is the improvement.
(ii) What is the average access time if the main memory is not interleaved? (5)
(b) Explain the concept of virtual memory. (5)

17. Write short notes on the following: (5+5)
(a) Vector processing
(b) Serial communication

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