CBCS SCHEME

USN 21CS34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With the help of a neat block diagram discuss the basic operational concept of a computer. **(08 Marks)**

b. Write a program to evaluate the arithmetic statement Y= (A + B) * (C + D) using three address, two address, one address and zero address instruction. **(08 Marks)**

c. Write the basic performance equation indicate the role of each parameter in the equation. **(04 Marks)**

OR

2 a. Define Addressing Mode. Explain the various addressing mode. **(10 Marks)**

b. With proper example explain Big - Endian and Little - Endian of byte addressing. **(06 Marks)**

c. What is performance measurement? Explain the overall SPEC rating of a computer. **(04 Marks)**

Module-2

3 a. With respect to handling interrupts from multiple devices explain:
(i) Interrupt nesting (ii) Dairy chain method. **(10 Marks)**

b. What is Bus arbitration? Explain centralized and distributed arbitration method with neat diagrams. **(10 Marks)**

OR

4 a. Illustrate a program that reads one line from keyboard, stored it in memory buffer and echoes if back to display in I/O interfaces. **(10 Marks)**

b. Discuss with a neat circuit diagram, the general 8 bit parallel interface circuit. **(10 Marks)**

Module-3

5 a. Explain the internal organization of 16-megabit DRAM chip configured as 2M × 8. **(08 Marks)**

b. With a neat figure illustrate the structure of synchronous DRAM (SDRAM). **(08 Marks)**

c. Discuss about any two types of Read Only Memory (ROM). **(04 Marks)**

OR

6 a. State the importance of cache memory and describe the different types of cache mapping techniques with diagram. **(12 Marks)**

b. With relevant figure explain organization of (1k × 1) memory chip. **(08 Marks)**

Module-4

7 a. With the help of logic diagram explain 4-bit carry look adder and its operation. **(10 Marks)**

b. Illustrate the hardware arrangement for sequential multiplication with an example. **(10 Marks)**

OR

8 a. Draw the single bus architecture and explain the control sequence for execution of instruction ADD (R3), R1. **(10 Marks)**

b. With neat sketches, explain the detailed organization of hardwired control unit. **(10 Marks)**

Module-5

9 a. With a suitable example explain the concept of pipeline processing. **(10 Marks)**

b. Draw and explain pipeline for floating point addition and subtraction. **(10 Marks)**

OR

10 a. With the help of flowchart and timing diagram explain four segment instruction pipeline. **(10 Marks)**

b. Explain the organization of SIMD array processor with an appropriate diagram. **(10 Marks)**

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