

EC - 601
B.E. VI Semester
Examination, December 2014
Industrial Electronics
Time : Three Hours

Maximum Marks : 70

- Note: i) Attempt one question from each unit.
ii) Each questions carry equal marks.

Unit - I

1. a) Draw and explain the block diagram of a power supply.
- b) What is a full-wave bridge regulator? Derive the expressions for rectifier efficiency and ripple factor for this rectifier.

OR

2. a) Draw and explain the working of a rt filter.
- b) What is a voltage regulator? Differentiate between fixed and adjustable voltage regulators. What are series and shunt voltage regulators.

Unit - II

3. a) Explain the constructional features and working principle of the SCR. How does it differ from a transistor? What is its two transistor analogy?
- b) Discuss the following with reference to SCR.
 - i) Break down voltage
 - ii) Forward current rating
 - iii) Finger Voltage
 - iv) Holding current
 - v) Latching current

OR

4. a) Enlist and explain the different methods of turn off of SCR.
- b) What is triggering of SCR circuits? Enlist and explain any one method of triggering of SCR circuits.

Unit - III

5. a) What are power diodes? Explain its types. What is reverse recovery time and reverse recovery current in power diodes?
- b) Explain the construction and volt-ampere characteristics of the IGBT.

OR

6. a) What are fast recovery diodes? Discuss it advantages and applications.
- b) What are the advantages and disadvantages of TRIAC over antiparallel SCR.

Unit - IV

7. a) What is an OP-Amp? What are the characteristics of an Ideal OP-. Amp?
- b) What is a window comparator? Explain its working.

OR

8. a) Draw and explain the frequency response of an OP-Amp. b) How can OP-Amp be used as a differentiator and integrator.

Unit - V

9. a) What is a PLC? Why is PLC an event driven device? What are the functions of PLC?
- b) What are the functions of input module and multiple modules in a PLC?

OR

10. a) What are the advantages and disadvantages of PLC over conventional relay controllers?
- b) Explain the ladder logic language.