BE (ETRT) SEM VIII (Rev) May 2013 20/5/13
D-SP. Proc. & Appli.

P4-RT-Exam.-Feb.-13-3-45

Con. 8837-13. **(REVISED COURSE)** **GS-3535**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Solve any **four** out of remaining **six.**
(3) Assume **suitable** data wherever **necessary.**

1. Explain briefly using appropriate diagrams wherever necessary :– **20**
   (a) Data and Program memory
   (b) Architectural differences between DSP processor and microprocessor.
   (c) Multiported memory
   (d) Special Addressing modes in P-DSP's.

2. (a) Discuss architectural features of TMS3206X. **10**
   (b) Explain what do you mean by pipeline depth and explain in what way this depth affects the pipeline performance. **10**

3. (a) What is Interpolation filter ? How can it be implemented using FIR filter ? **10**
   (b) List on-chip peripherals and their functional requirements in C5X series of digital signal processor. **10**

4. (a) Explain Interrupt Mask Register and Interrupt Flag Register of C5X. **10**
   (b) Discuss salient features of ADSP21XX series DSP processor and its functional blocks. **10**

5. (a) How does clock speed (crystal) affect the system through put in a typical controller based system ? What are the techniques used by designers to retain high through put at lower crystal speed ? **10**
   (b) What are various functional units of C54X CPU ? Explain in detail the function of compare, select and store unit (CSSU) and exponent encoder. **10**

6. (a) Discuss salient features of Motorola DSP 563XX. **10**
   (b) What are the various P-DSP families and their applications ? Discuss various factors to be considered while choosing DSP Processor. **10**

7. Write short notes on (any **two**) :– **20**
   (a) Implementation of FIR and IIR filters using C54X processor
   (b) Role of interrupt pins in a DSP device
   (c) FFT algorithm using typical DSP.
