S7 EC K15F 0300

NOV 2015

Reg. No.: .....

Name : .....

VII Semester B.Tech. Degree (Reg./Supple./Improve. – Including Part Time) Examination, November 2015

(2007 Admn. – Onwards)

PT 2K6/2K6 EC 701 : MICRO ELECTRONICS TECHNOLOGY

Time : 3 Hours Max. Marks : 100

PART – A

1. a) Explain subtractive etching and additive etching with neat diagrams. 5

   b) Describe the possible defects in epitaxial growth. 5

   c) Draw the schematic of a simple Biomos inverter and explain its operation. 5

   d) What is sub threshold conduction and DIBL effect ? 5

   e) What are stick diagrams ? Give the encodings for a simple nMOS process ? 5

   f) List the various λ based design rules adopted for the transistor in nMOS, PMOS and CMOS. 5

   g) Briefly describe scattering in nano transistors. 5

   h) Briefly explain electron spin transport. 5

PART – B

2. Explain CVD process for Si in detail with neat diagram. 15

OR

3. i) Explain the Deal-grove model of formation of SiO_2 and analyse the prediction of oxide thickness. 10

   ii) List the effects of crystal defects in semiconductor fabrication. 5

P.T.O.

4. i) Derive the expression for Ids in a nMOS transistor in the different regions of operations. 10

   ii) Mention the types of nMOS transistors and give their output characteristics and parameters. 5

OR

5. i) What are hot carrier ? 5

   ii) How hot carriers affect the performance of BJT and MOS ? 10

6. i) Give the stick diagram of the logic function X = A + B.C using nMOS stick layout design style. 10

   ii) Draw the stick diagram of CMOS inverter. 5

OR

7. Give the nMOS implementation of Sum and Carry output of a half adder circuit ? Draw the layout of the above circuits. 15

8. Write short notes on : 15

   i) Junction Isolation and Trench Isolation.

   ii) Ballistic nano transistors. 15

OR

9. i) Explain the SWAMI Process in detail with appropriate diagrams. 10

   ii) Write about the Ohms law in nanometer scaled devices. 5
