(DEE 215)

B. Tech. DEGREE EXAMINATION, MAY - 2015

(Examination at the end of Second Year)

ELECTRICALS AND ELECTRONICS

Paper - V : Digital Electronics

Time : 3 Hours **Maximum Marks : 75**

Answer question No. 1 compulsory ***(15)***

Answer ONE question from each unit ***(4 x 15 = 60)***

1) a) Convert $(11\ 011\ .\ 101)_2$ into decimal.

b) Subtract $(111\ 001)_2$ from $(101011)_2$ by using 2's complement method.

c) What are "Universal gates". Why they are called as Universal gates?

d) Draw the symbol, Truth table of EX. OR & EX-NOR gates.

e) Draw the circuit of CMOS NAND gate.

f) Apply the De-Morgan's theorem & simplify $\overline{\overline{A+B}+\overline{CD}}$

g) Define the need for Registers.

h) Minimize the expression $Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$ using K. Map method.

i) Find the ASCII value of DIGITAL ELECTRONICS

j) Define combinational circuit.

k) List the applications of counters.

l) Draw the logic diagram & truth table for SR latch.

m) Define POS form.

n) Why binary numbers are used in Digital Systems?

o) Draw the circuit of RTL basic NOR gate.

Unit – I

2) a) Convert the following decimal numbers into binary, octal & Hexadecimal.

i) 255 ii) 1023

iii) 65,535 iv) 4097

b) Convert the following binary numbers to gray code

i) 10101100

ii) 1110011

iii) 10010010

OR

3) a) Prove using De Morgans theorems that XOR & XNOR are complements to each other.

b) Prove that if a & b are switching variables then prove that $a + b = a \oplus b \oplus ab$.

Unit – II

4) a) Present the steps involved in the design procedure of a combinational circuit. Consider a suitable example.

b) Design 3 × 8 Decoder and list out its applications.

OR

5) a) Draw the block schematic & truth table for full-subtractor. Explain the design approach for full-subtractor with 2 half-subtractors. Draw the relavent logic diagram with necessary expressions.

b) Draw & explain the operation of look ahead carry adder.

Unit – III

6) a) Realize on SR latch circuit using

i) NOR gates.

ii) NAND gates. Give truth tables.

b) Convert a D flip – flop to JK flip- flop & to T flip-flop

OR

7) a) Implement the given Boolean function using 4 × 1 multiplexer

$F(A,B,C,D) = \Sigma m(2, 5, 8, 9, 10, 14, 15)$

b) Design, draw & explain 4 – i/p priority encoder.

Unit – IV

8) a) Discuss about synchronous & ripple counter. Compare their merit & demerits.

b) What do you mean by universal shift registers? Draw & explain it circuit diagram & Operation.

OR

9) a) Explain about TTL logic.

b) Write a short notes on sequential programmable devices.

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