Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH/CSE(N)/IT(N)/SEM-3/CS-303/2012-13

2012

COMPUTER ORGANIZATION

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives from the following :

$10 \times 1 = 10$

i) Maximum number of directly addressable locations in the memory of a processor having 10 bits wide control bus, 20 bits address bus and 8 bit data bus is

a) I K b) 2 K

c) 1 M d) None of these.

ii) With 2's complement representation, the range of values that can be represented on the data bus of an 8 bit microprocessor is given by

a) – 128 to + 127 b) – 128 + 128

c) – 127 to ≠ 128 d) 0 – 255.

iii) Which of the following addressing modes is used in instruction RAL

a) Immediate b) Implied

c) Direct d) Register.

iv) The principle of locality justifies the use of

a) Interrupts b) polling

c) DMA d) Cache memory.

v) Periodic refreshing is needed

a) SRAM b) DRAM

c) ROM d) EPROM.

vi) Subtractor can be implemented using

a) adder b) complement

c) both (a) and (b) d) none of these.

vii) Physical memory broken down into groups of equal size is called

a) page b) tag

c) block / frame d) index.

viii) Bi-directional buses use

a) Tri-state buffers

b) Two tri-state buffers in cascade

c) Two back to back connected tri-state buffer in parallel

d) two back to back connected buffers.

ix) Micro Instruction are kept in

a) Main memory b) Control memory

c) Cache memory d) None of these.

x) Instruction cycle is

a) fetch-decode-execution

b) decode-fetch-execute

c) fetch-execution-decode

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Explain the difference among three-address, two address, one address and zero address instruction for the equation $X = (A + B)^* C$.

   b) Explain Base-Index Addressing with proper example.

   (4 + 1) = 5

3. A disk drive has 20 sectors/track, 4000 bytes/sector, 8 surfaces all together. Outer diameter of the disk is 12 cm and inner diameter is 4 cm. Inner-track space is 0.1 mm. What is the no. of tracks, storage capacity of the disk drive and data transfer rate there from each surface ? The disk rotates at 3600 rpm.

4. What is a Von Neumann architecture ? What is Von Neumann bottleneck ? (3 + 2) = 5

5. What do you mean by Stack memory.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. a) Draw a diagram for digital computer.

   b) What is bus ? Draw and describe the bus architecture for a digital computer.

   c) What are difference between Serial and Parallel transmission ? 4 + 7 + 4

7. a) Explain Booth's algorithm for multiplication of signed 2's complement number in flow chart.

   b) Apply Booth's algorithm to multiply the two numbers $(6)_{10}$ and $(-9)_{10}$. Assume the multiplicand and multiplier to be 5 bits each.

c) Explain the relative advantages & disadvantages of parallel adder over serial adder.

d) What is virtual memory ? 5 + 4 + 4 + 2

8. a) What is Cache memory ? Why is it needed ?

b) Explain the Write-through and Write-back mechanism ?

c) Given the following, determine the size of the sub fields (in bits) in the address for Direct Mapping, associative and Set associative mapping cache schemes :

We have 256 MB main memory and 1 MB cache memory.

The address space of this processor is 256 MB.

The block size is 128 bytes.

There are 8 blocks in a cache set.

d) A three-level memory system having cache access time of 5 nsec and disk access time of 40 nsec, has a cache hit ratio of 0.96 and main memory hit ratio of 0.9. What should be the main memory access time to achieve an overall access time of 16 nsec ? (2 + 1) + 2 + 5 + 5)

9. a) What are the different types of DMA controllers and how do they differ in their functioning ?

b) What is instruction cycle ? Draw time diagram for memory read operation.

c) How does work polling ? (7 + (1 + 4) + 3)

10. Write short notes on any *three* of the following : 3 × 5 = 15

i) Addressing modes

ii) Bus organization using tristate buffer

iii) Paging

iv) Microinstruction.