M 23316

Reg. No. : .....

Name : .....

VI Semester B.Tech. Degree (Reg./Sup./Imp. – Including Part Time) Examination, May 2013
(2007 Admn. Onwards)
PT2K6/2K6EC 606(A) : DESIGNING WITH VHDL

Time : 3 Hours Max. Marks : 100

***Instruction** : Answer **all** questions.*

1. a) State the rules for writing an identifier. 5
   b) What is a sensitivity list ? 5
   c) What are packages ? 5
   d) What are procedures ? 5
   e) Describe the approaches for creating test benches. 5
   f) Define a s–a–o fault. 5
   g) How do you identify a buried node in a CPLD ? 5
   h) What is FPGA ? 5

2. a) What are the different data types used in VHDL ? Explain with examples. 15

   OR

   b) What are the different ways of writing the architecture of VHDL program ? 15

3. a) Using generic, design a set of registers with asynchronous reset and load. 15

   OR

   b) With an example, show how an operator can be overloaded in VHDL. 15

4. a) Design a circuit in VHDL that can detect 101 in a given sequence of input. 15

   OR

   b) Write a test bench program for a 3 bit up counter with preset and clear. 15

5. a) Write a short note on metastability resolution time. Explain the different methods by which this can be implemented in the circuit. 15

   OR

   b) With an example in VHDL, show how a Moore machine is different from a Mealy machine. 15