B.E./B.TECH.(FULL-TIME) DEGREE END SEMESTER EXAMINATIONS, APRIL/MAY 2014
ELECTRONICS AND COMMUNICATION ENGINEERING
VI SEMESTER
EC 9355 DIGITAL VLSI
(Regulation 2008)

Time:3 Hrs **Max Marks:100**

Answer all questions
Part-A (10 X 2=20 Marks)

1. Find the operating region of MOSFET (linear, saturation, velocity saturation) biased with V_{GS} = 1.5V, V_{DS} = 2V, V_{DSAT} = +0.6V, V_T = +0.4V.
2. For the inverter circuit shown in Fig.1 give the expression for the energy drawn from supply V_{DD} to charge capacitor C_L.

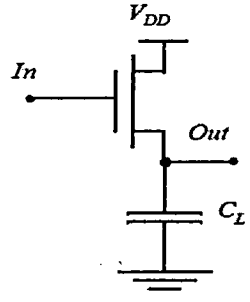
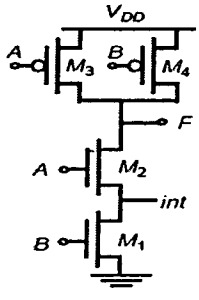
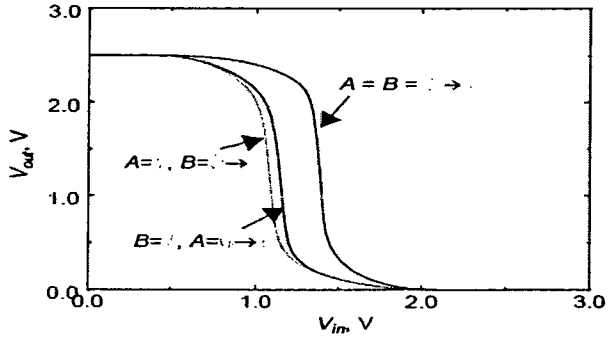


Fig.1

3. Implement the Boolean function $\overline{Y}$ = AB + C using pass transistor logic.

4. The circuit given below is the 2-input static CMOS circuit and its VTC (Voltage Transfer Characteristics) is shown on the right. Denote the combination of inputs on the curves.





5. Discuss clock skew and clock jitter.

6. For the memory circuit shown in Fig.3, determine the bit line values BL[0],BL[1],BL[2],BL[3], if the address is given as
WL[0]=0,WL[1]=1,WL[2]=0,WL[3]=0.

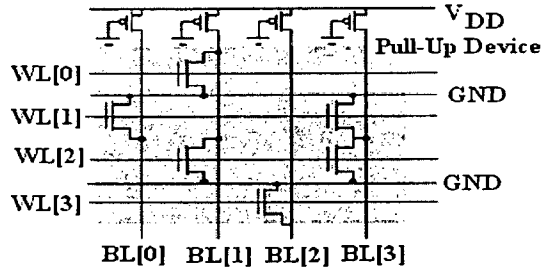


Fig. 3

7. Sketch the circuit used to generate the next carry using the dynamic logic circuit.
8. Draw the circuit schematic of 2 bit barrel shifter.
9. What is CPLD and how is it different from other PLDs?.
10. Sketch the structure of Interconnect Switch used in Xilinx FPGA to connect different blocks.

PART - B (5 x 16 = 80)

11. . i. Determine V_{OH}, V_{OL}, & V_M, for the inverter in Fig.4 (4)

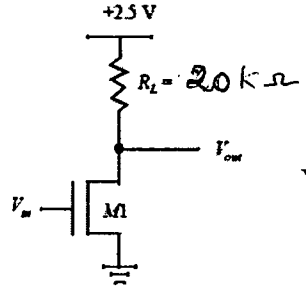


Fig.4

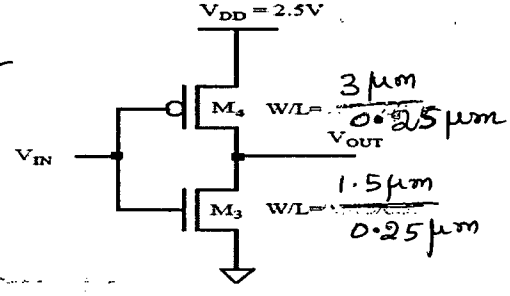


Fig.5

ii. Find V_M, and V_O, for the inverter shown in the Fig.5 (6)

NMOS:V_{Tno} = 0.4V, Kn' = 115 µA/V^2 ,V_{DSAT} = 0.6V, λ= 0.06V^{-1}, γ = 0.4V$^{1/2}$, $2\varphi_F$ = -0.6V
PMOS: V_{TPo} = -0.4V, Kp' = -30 µA/V^2, V_{DSAT} = -1V, λ= -0.1V^{-1}, γ = -0.4V$^{1/2}$, $2\varphi_F$ =0.6V

(iii) Derive equations to show the current-voltage relationship of NMOS transistor in various operating regions. (6)

12. a. i) Implement the equation Y = A' + AB' + BC' + CD' using static CMOS logic and Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 1/1 and PMOS W/L = 2/1. (6)

ii. Find the switching power dissipation of the combinational circuit given in equation 12.a.i, considering the occurrence of inputs as independent with probabilities P(A=1)=0.5, P(B=1) =0.25, P(C=1)=0.15, P(D=1)=0.10. Assume VDD=1.8V, Cout=150fF and fclk=2MHz. (5)

iii. In Domino logic, the presence of an inverter tempt us to remove the evaluation transistor to offer reduced load to the clock input. Can this be done? If not explain the reason. (5)

OR

12.b.i. List out the signal integrity issues in dynamic CMOS logic design and explain any two issues in detail. (10)

ii. The pass transistor implementation of 2 input AND gate is shown in Fig.6 along with its Voltage Transfer Characteristic curve. Denote the combination of inputs on the curves and explain the behaviour of the curves for different combination of inputs. (6)

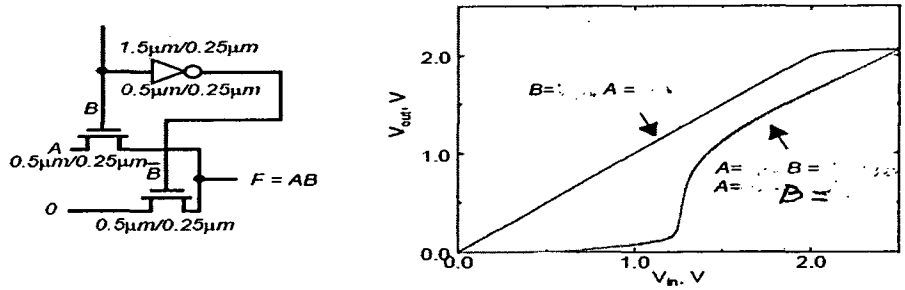


Fig.6

13.a.i. Design MUX based negative edge triggered register and express its setup time, hold time and $t_{c\text{-}q}$ delay. (8)

ii. Design a 4 x 4 NAND ROM for storing the following contents. (8)

WL_0 = 1 1 0 0
WL_1 = 0 0 1 1
WL_2 = 1 0 1 0
WL_3 = 1 0 0 1

OR

b.i. Implement the Master Slave register using C^2MOS logic and explain how the problems due to 0-0 and 1-1 overlap of clock signals are overcome. (8)

ii. How will the circuit operation of the circuit shown in Fig.7 get affected if the transmission gates are replaced with NMOS pass transistor. (8)

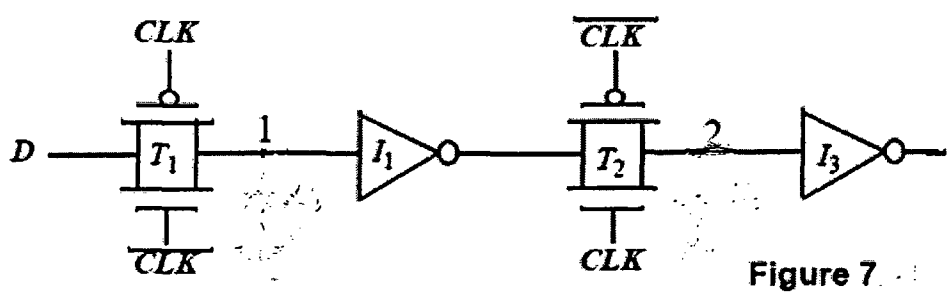


Figure 7

14.a.i Design full adder using Mirror Adder Architecture. (8)

ii. Design 4 x 4 Wallace Tree Multiplier. (8)

OR

b. i. Explain the concept behind the Linear Carry Select Adder. Also design a 16 bit adder using Linear Carry Select Principle and give the best case and worst case time delays. (8)

ii. Give the drawback involved in Linear Carry Select Adder and explain how this is overcome using Square Root Carry Select adder. (8)

15.a. i. Draw and explain the salient features of configurable logic block (CLB) of XC4000 FPGA. (10)

ii. Draw the internal architecture of ACT1 Logic Module and use it to implement the logic function $F=(A\cdot B) + (B'\cdot C) + D$ using Shannon's Expansion Theorem. (6)

OR

b. i. Explain Logic cell architecture of Altera device. (6)

ii. Write detailed notes on any 2 of the following.

a. Gate Channel Capacitance and Junction Capacitance (5)

b. Techniques to reduce the glitches in logic circuit. (5)

c. Stick diagram with a typical example. (5)