BE | ETRX | VIII (Rev) 15/5/2012

A. VLSI Design

SA 1st half 131

Con. 3636-12. (REVISED COURSE) GN-7436

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1 is compulsory.**
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any suitable data whenever required and justify the same.

1. a) Explain metal migration in interconnect. 5
b) Explain programming techniques of EEPROM using hot electron and Fowler-Northeim emission. 5
c) If the width and length of the interconnect is reduced by 30%, then the propagation delay of an interconnect will increase or decrease, by how much %? 5
d) Draw and explain manchester carry out circuit using carry kill bit. Also draw 4-input dynamic Manchester carry chain circuits. 5

2. a) What would be the conductor width of power and ground wires to a50 MHz clock buffer that drives 100 pF of on-chip load to satisfy the metal-migration consideration (J_{AL} = 0.5mA/μm)? What is the ground bounce with chosen conductor size? The module is 500 μm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1ns. (Assume sheet resistance of wire = 0.05Ω/sq). 10
b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. 10

3. a) Give and explain the drawback with ripple carry adder. Explain 4-bit CLA adder with its carry equations, logical network and writs its Verilog description. 10
b) Explain how ESD (electro-static discharge) affect the MOSFET. Give and explain input protection circuits. 10

4. a) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10
b) Draw 4 X 4 pseudo-nMOS ROM array circuitry having stored following data. 0011, 1010, 1100, 0101. Also list the no. of address pins, data pins and word lines. 10

5. a) Explain the need of frequency compensation in CMOS operational amplifier. 10
b) Give and explain single phase clock system and explain its drawback. 10

6. a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. 10
b) What is cross talk in IC's? Explain various methods to reduce it. 10

7. Write short notes on (any three): 20
a) Low power design consideration.
b) Reliability issues in CMOS circuits.
c) Carry save adder.
d) Switch capacitor amplifier.