FACULTY OF INFORMATICS

B.E. 3/4 (IT) II-Semester (Old) Examination, May 2013

Subject : Advanced Computer Architecture
(Elective – I)

Time : 3 Hours   **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Sketch the architecture of a vector super computer.   (3)
2. Define Network throughput and Hot spot.   (2)
3. Define Vector processor.   (2)
4. List primitive operations for AI based symbolic processors.   (3)
5. State cache coherence problem.   (3)
6. What is Latency-Hiding?   (2)
7. What is Data-Parallelism?   (2)
8. List control constructs for specifying parallelism.   (3)
9. Define Binary Spin Lock.   (3)
10. Define Optimistic concurrency.   (2)

PART – B (5x10=50 Marks)

11. (a) Compare Data flow and control flow computers.
    (b) List and describe factors that affect Network performance.

12. Describe the following processor families in the Design space in terms of clock Rate and Cycles per Instructions.
    (a) Scalar CISC
    (b) Super scalar RISC
    (c) Vector sueprcomputer
    (d) Super pipelined processor

13. Explain Routing in Omega Networks.

14. Describe compilation phases in parallel code generation.

15. Describe principles of various synchronization mechanisms for inter-process communications.

16. Write a note on Software Parallelism and Hardware Parallelism.

17. Describe pipeline Instruction processing.

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