FPGA-based Switched Reluctance Motor Drive and DC-DC Converter Models for High-Bandwidth HIL Real-Time Simulator

(I)

Topic 18: Electrical systems in road vehicles

18h. Modeling, simulation and design methods, reliability issues

Lecture Presentation

Abstract

In this paper, we describe an FPGA implementation of a Switched Reluctance Motor Drive (SRM) and a DC-DC bidirectional boost converter targeted for Hardware-In-the Loop (HIL) testing of modern SRM controllers. These FPGA models allow the HIL simulation of SRM drive and boost converter with switching frequencies in the 50-100 kHz range because of the very high sampling rate of the FPGA. The models are also integrated into the RT-LAB real-time environment and directly linked with the simulator I/Os, providing ultra-low HIL gate-in-to-current-out latency, suitable for the testing of modern motor controllers.

Synopsis

As of 2012, it's a very common industrial practice to validate motor drive control with Hardware-In-the-Loop (HIL) simulation[1][2]. The advantages of this are numerous. For example, the real-time simulated motor drive can be tested with borderline conditions that would damage a real motor prototype. With ever decreasing time-to-market time, HIL simulation enables engineers to design the motor control *in parallel* to the motor drive itself. Hybrid electric vehicle (HEV) OEMs and other motor drive manufacturers use HIL technology to speed up development time by allowing early error detection before conducting tests on physical prototypes. At the production stage, HIL simulation can also be used to verify code integrity at controller software releases with automated correlation tests.

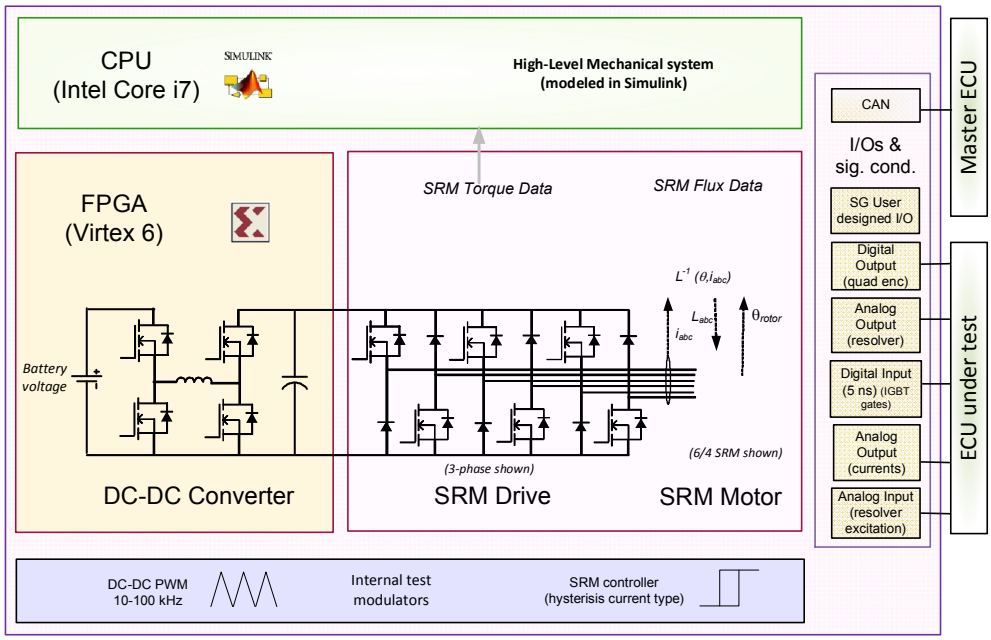

Fig. 1 FPGA-based SRM Drive HIL simulator with DC-DC converter

In the field of HEV, permanent magnet synchronous motors (PMSM) are the preferred choice of many manufacturers, mainly for efficiency reasons. The interest in switched reluctance motor drive is currently increasing also because of its low manufacturing costs, rugged construction and simplicity of controller design. Since the rotor has no windings and no magnets, it is a good candidate for drive operation at high speed and in adverse environments. As with the PMSM, a real-time simulator is the ideal tool to conduct research on this relatively new application of the SRM. Sensorless drive designs and control optimisations, for example, pose challenges that can be tackled efficiently with a real-time simulator.

Advances in power electronics have made possible the design of very high switching frequency motor drive and power converters. The SRM drive, with its high speed capability, can require switching frequencies reaching 20 kHz. Modern HEV topologies with voltage boosting stage goes further with DC-DC converters with PWM frequencies up to 100 kHz.

The HIL testing of such devices therefore requires a real-time simulator with a very high sampling rate, well below 1µs to obtain reasonable accuracy at 100kHz. FPGA-based SRM drive and DC-DC converters are an excellent solution to this challenge. In this paper, we detail such a model implemented on a Virtex-6 FPGA chip within the RT-LAB real-time system. It is, to our knowledge, the first industrial FPGA-based SRM Drive HIL simulator described in the literature.

HIL simulator model components

The FPGA implementation SRM Drive HIL test system in the RT-LAB real-time simulator is depicted in Fig. 1. It has 6 main components:

SRM motor: currently supported model is the 6/4, 10/8 and 12/10 configurations. 6/4 means a SRM with 6 poles on the stator and 4 poles on the rotor. It also supports multiple of these (ex: 12/8) with stator phases connected in parallel.

SRM inverter: an IGBT inverter with 2 IGBTs (with anti-parallel diode) and Diode per SRM phase.

Bidirectional DC-DC boost converter: an H-bridge with 4 IGBTs (with anti-parallel diode) to boost the battery voltage before the SRM inverter.

Internal test modulators: to enable stand-alone testing of the different FPGA modules without an external controller connected to the simulator. The SRM drive modulator is a current-control hysteretic controller while the DC-DC converter modulator is of PWM type. These modulators are unused when the simulator is running with a controller connected to the I/Os.

I/O modules: enable the user to map the external simulator I/O signals to the model signals.

CPU model interface: allows the user to interface other models on the CPU to the FPGA models. In a complex HEV system, for example, the mechanical equation would be computed on the CPU from the different model torque contributions: SRM electric torque, ICE torque, transmission, road friction, etc…

Of special importance are the latencies of the different modules. From the controller point of view, the latency from the gate sampling at the digital input of the simulator to the output of the current at the analog output (SRM or DC-DC drive) must be minimal, under 1 µs in some applications. Also, the model sampling frequencies should be at 100 higher than the PWM frequency in use (i.e. for 1 % precision).

ML605 Virtex-6 FPGA cards are used in the current implementation of these models with a 200 MHz clock. On the RT-LAB simulator, these FPGA cards are directly connected to fast 16 D/A converters with a *simultaneous* conversion rate of 1 µs.

Module	Sampling rate/Latency (ns) (not including D/A)
SRM inverter	50/100 ns
SRM motor (6/4)	50/100 ns
DC-DC Boost converter	120/120 ns

Switched Reluctance Motor modeling

This SRM model integrates its flux at each winding, considered as uncoupled in this model[3][4][5]. The model working equation is:

$$\int (V_{abc} - R_s I_{abc})dt = \psi_{abc} \qquad (1)$$

where I_{abc} is the stator current inside the winding, R_s is the stator resistance and V_{abc} is the voltage across the stator windings. The current is then derived from the machine flux characteristics $\psi_{abc}(I,\theta)$ and stored in tables on the FPGA.

In the SRM, there is a three-dimensional relationship between excitation current, rotor position and flux linkages. This flux relationship can be found using commercial FEA software like JSOL's JMAG-Studio or Infolytica's MotorSolve. Fig. 2 shows this flux relationship and the corresponding FEA analysis using MotorSolve for the 12/8 SRM used for example in this paper.

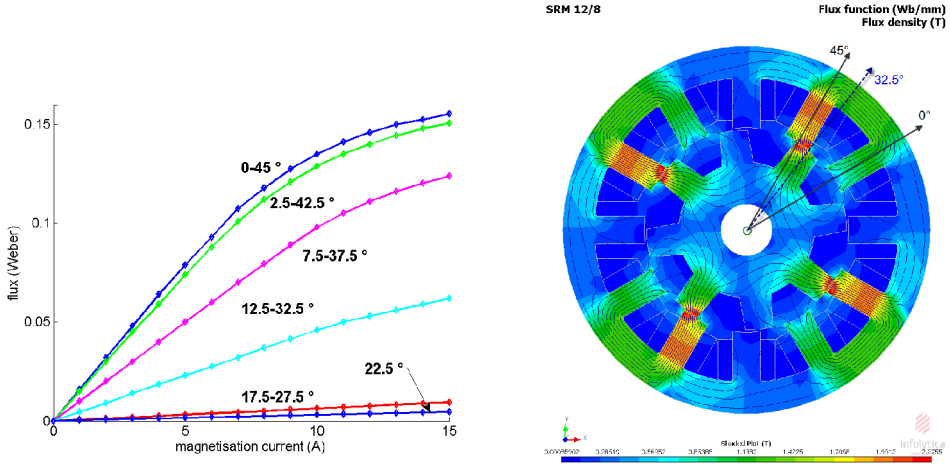

Fig. 2 Left: Three-dimensional relationship between excitation current, rotor position and flux linkages for 12/8 SRM motor Right: FEA analysis on the 12/8 SRM in MotorSolve.

From this flux $\psi(I,\theta)$ relationship, the Opal-RT model derives the inverted characteristic $I(\psi,\theta)$, using spline methods[6][7]. This inverted characteristic is shown in Fig. 3. Note the 'electric' angle scale from 0 to 90° in the figures because a 12/8 SRM is electrically equivalent to a 6/4 SRM.

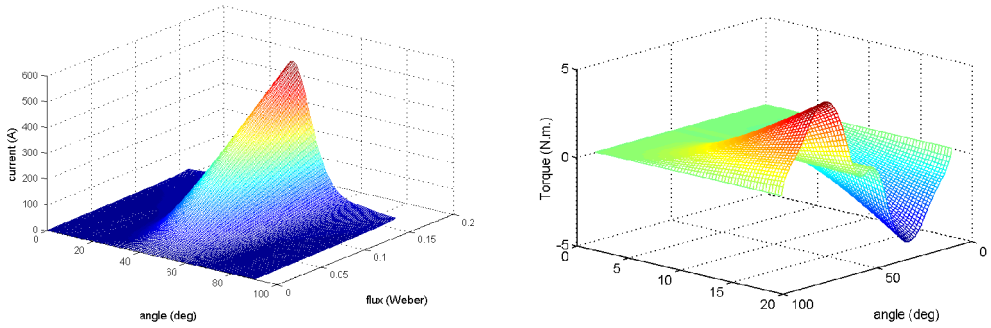

Fig. 3 Inverted Current characteristic (left) and torque characteristic (right).

The produced electrical torque is also derived from the flux-current characteristic, pre-computed and stored in tables prior to the real-time simulation. The torque is computed by integration and derivation of the machine co-energy W_c using Eq. (2). For the same motor again, Fig. 3 shows the torque characteristic obtained.

$$T_e(I,\theta) = \frac{\partial}{\partial\theta} W_c(I,\theta) \qquad W_c = \int_0^i \psi(I,\theta)dI \tag{2}$$

The SRM motor model uses of Time-Domain-Multiplexing (TDM) in the solver design. TDM pipelines the equations of the motor (integration, addition, etc…) into a serial sequence of arithmetic operators and results in very low sampling times. Pipelining, however, induces a latency that is greater than the sampling time.

DC-DC boost converter modeling

The DC-DC converter was designed with a state-space approach with 2 states (inductance current and capacitor voltage) with pre-calculation of the 16 combinations of the 4 IGBT's conduction states.

The model consequently supports all modes, normal and faulty. Also, with the state-space approach, the model latency is equal to its sample time of 120 ns. This sample time also determines the resolution of the IGBT gate at the simulator I/Os. With a 120 ns sampling time, the DC-DC converter precision with regards to gate sampling is 1.2% for example.

SRM inverter modeling

The SRM inverter was designed using a switching-function approach with high impedance capability [1]. The main reason for this choice was to minimize the model sampling time and time resolution. The model was implemented using Time-Domain-Multiplexing (TDM) method in the solver design with the same benefits and limitations that are found in the SRM motor design.

Model validations and tests

The FPGA SRM motor drive and DC-DC converter models were developed with SimPowerSystems v5.5 (MATLAB R2011B) used as a reference. Static and dynamic tests were performed and showed an excellent match. We show only the dynamic tests in this paper.

The tests were conducted on the HIL system with the internal test modulator and the waveforms were captured at the simulator analog outputs by an oscilloscope. We compare these results with the ones obtained offline in SimPowerSystems.

<u>DC-DC boost converter model validation</u>

The dynamic response of the FPGA DC-DC converter was tested on-chip and compared with offline simulation using SimPowerSystems. The on-chip waveforms were captured with an oscilloscope and are show in Fig. 4 together with the SPS results. All parameters are shown in the figure. The test consisted in charging the load current from -10A to +40A (with load current defined as going out of the converter). A PWM frequency of 50 kHz a duty cycle of 20% and a deadtime of 1 µs are used. Initial current of ~ -60A final current of ~160A are found in both on-chip and offline simulations. Capacitor voltage also saturates correctly to 0 V in both case. Oscillation frequency and damping match well also.

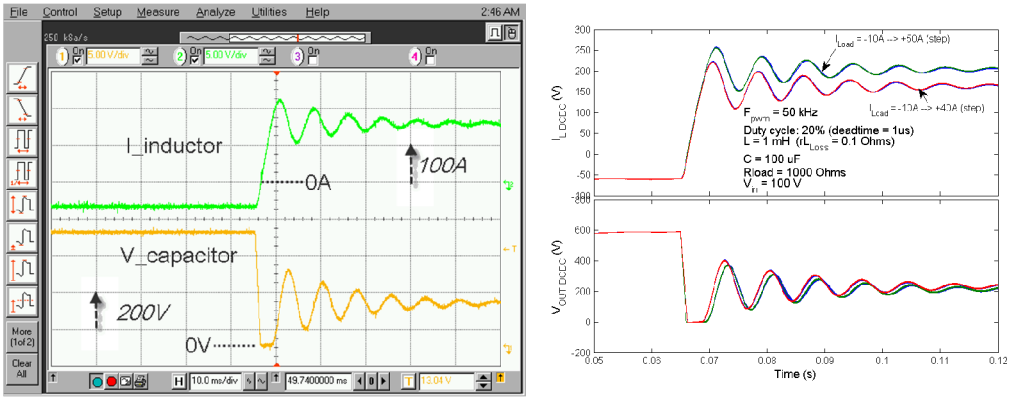

Fig. 4 DC-DC converter load step. FPGA on-chip results (left) vs. SPS offline simulation (right)

SRM Drive model validation

The SRM drive was also implemented on the ML-605 FPGA chip. The tested SRM motor parameters are described in the previous sections. The SRM windings have a resistance of 0.63 Ohms. For the purpose of the test, we ran this 12/8 SRM motor at 2500 RPM. The DC link voltage is set to 300 volts and the FPGA internal current controller is used with current command stepping from 5 to 10 A and turn on turn off angles of 20° and 43.5° respectively. Again, the model results were captured with an oscilloscope and compared with offline simulation in Fig. 5. The general behavior of the models is similar: similar band gaps of currents, same current overlap near 0 Amp, switching frequency that decreases after a phase is turned-on as the inductance increases due to the alignment of rotor and stator poles. Torque also matches well but is not shown here due to lack of space.

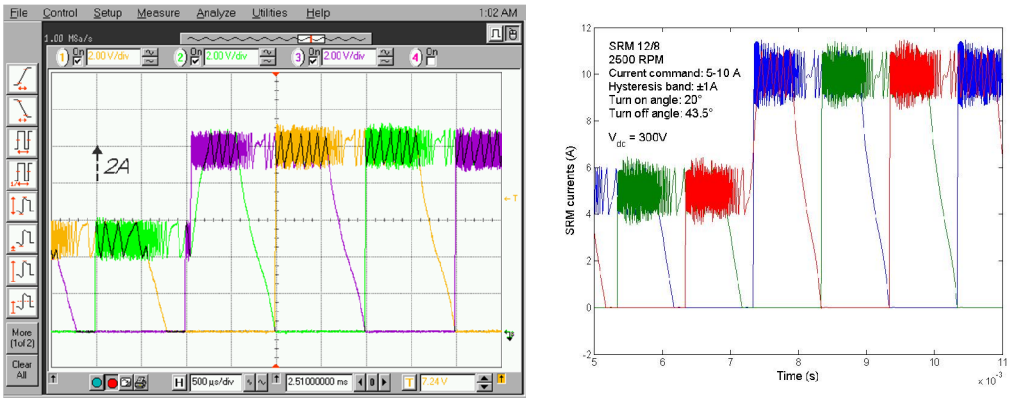

Fig. 5 SRM Drive current command step: FPGA results (left) vs. SPS offline simulation (right)

Conclusion and final paper contents

The final paper will contain further validation of the SRM drive and DC-DC boost converter. The model is due for delivery to a client in Japan in the 1st quarter of 2013. We should then be able to obtain HIL results with the client controllers connected to the real-time simulator. *As mentioned in the paper, this HIL test system of SRM drive based on FPGA is the first one reported in the literature.*

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