Digital VLSI Design Note

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Branch - ETC

Sem - 5th

Module-1   chapter-1

Introduction : Historical perspective, VLSI design methodologies, VLSI Design Flow, Design Hierarchy, Concept of Regularity, Modularity and Locality, VLSI design styles, Computer-Aided Design Technology.

BOOKS : CMOS digital integrated circuits, Analysis and Design, by Sung-Mo Kang and Yusuf Lablebici

NPTEL : VLSI design by S. Dasgupta, IIT Roorkee

Moore's law :- (Gordon Moore)

→ This law states that, the no. of transistors in a particular ~~integ~~ chip doubles every 2 years.

→ Later on Moore's modified it by observing the increase in transistor count and proposed that no. of transistors are doubled in a chip every 18 months.

→ Increase in transistor counts leads to decrease in transistor size or inface the gate length of MOSFET.

Objective of VLSI Design :-

→ There are 3 main objectives of any VLSI Design. The design should

(i) consume less area → small size gadget

(ii) High speed of operation → Less delay in ckt

(iii) Low power consumption → better battery life.

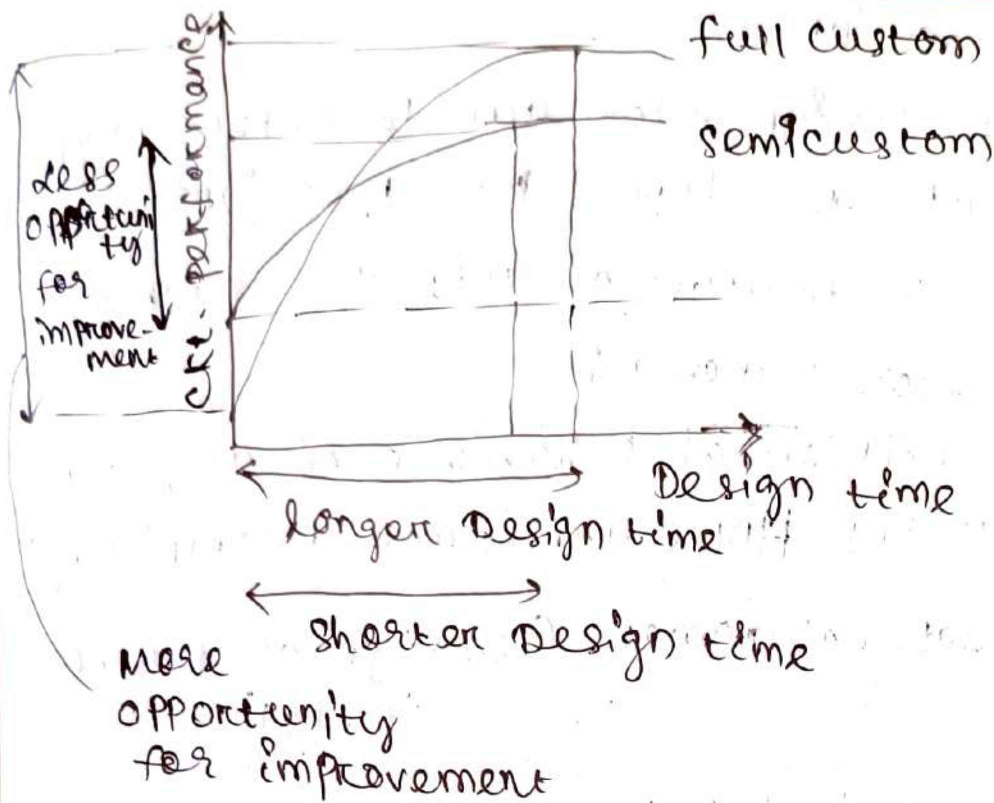
→ Apart from this the design should be in such a way that the device should be reliable. (TRUST)

VLSI Design methodology :-

→ Depending on the time to deliver the product and to market and design complexity there are two methology for VLSI design.

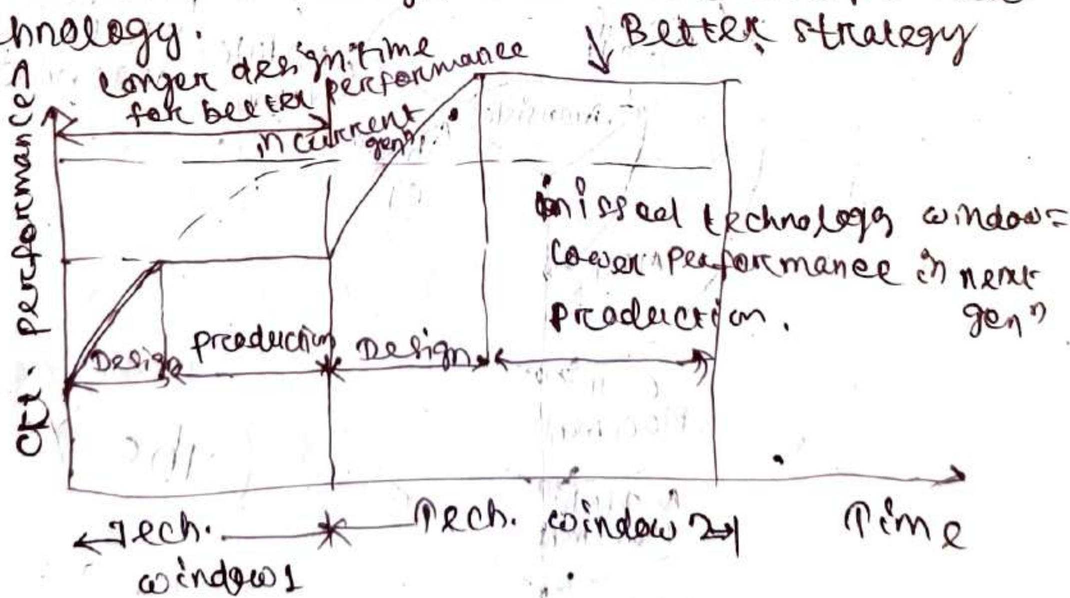
(i) Semicustom design
(ii) Full custom design

Semicustom Design	Full custom Design
(1) In this case we design in software level and implement it in readymade available hardware like FPGA, CPLD, Gate Array etc.	(1) We start designing the circuit from transistor level and fabricate it.
(2) Hardware description languages like Verilog, VHDL etc. are used to write the program.	(2) Layout design tools are used.
(3) The level of optimization is less and mainly done by the tool.	(3) The geometry and the placement of every transistor can be optimized individually.
(4) Time to deliver to market is less.	(4) Time to deliver to market is more.
(5) Design time is less.	(5) Design time is more
(6) Lowest circuit performance	(6) Better circuit performance.
(7) Less costly	(7) More costly



→ The selection of design methodology depends on the performance requirement, technology being used, expected lifetime of the product and cost of the project.

→ The better strategy in VLSI industry is to have less design time and adopt new technology.



VLSI Design flow:

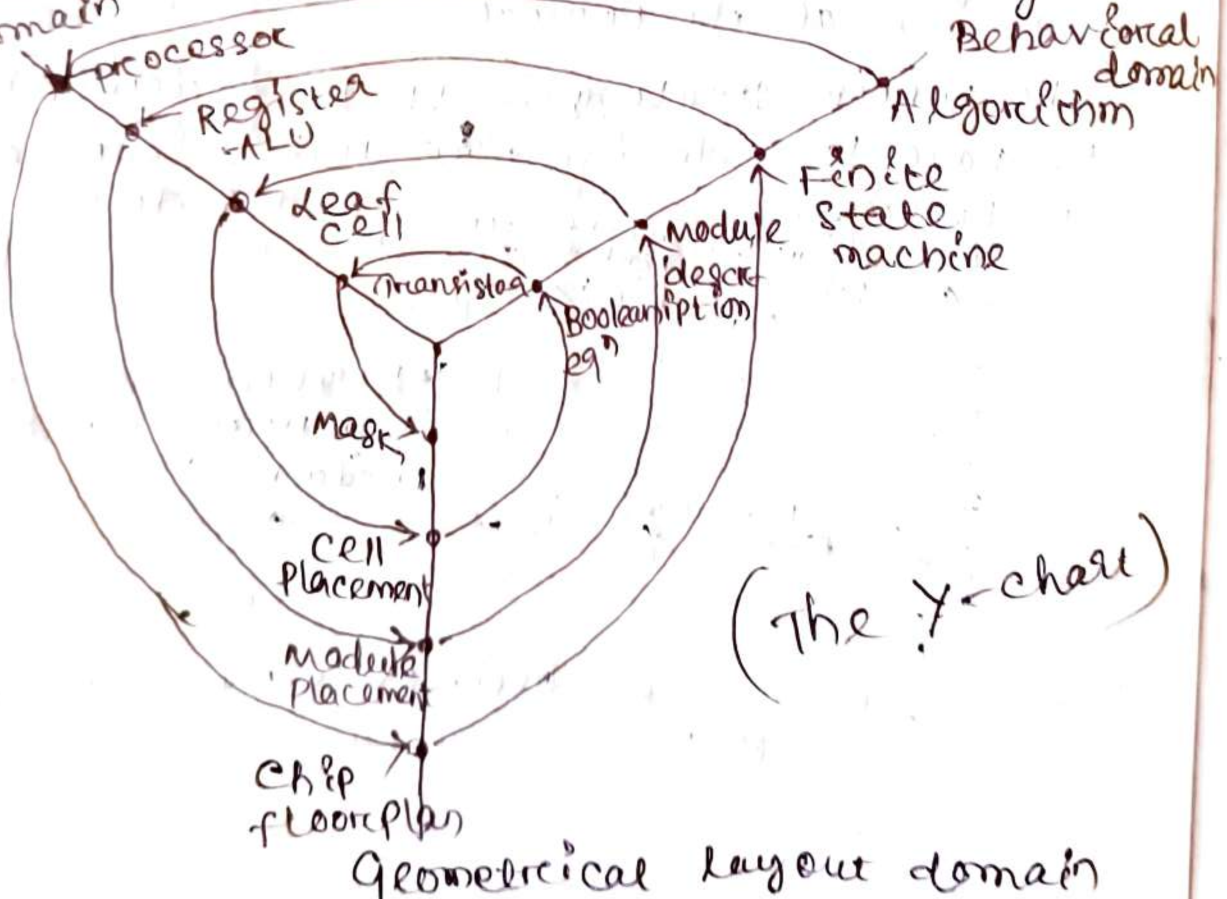
→ The VLSI design flow can be represented by Y-chart developed by D. Gajski.

→ There are 3 domains of this flow such as

(1) Behavioral domain
(Description of behaviour of any ckt. using HDL (Hardware descrip? lang.)

(2) Structural domain (Design of parents module)

(3) Geometric or layout domain
(Here layout of the whole ckt starting from transistor level to design)



(The Y-chart)

→ Design of a VLSI chip starts from behavioral domain where specification of the chip are defined.

→ specification means the functionality, operating conditions, time of operation etc. are decided before designing a chip.

→ The architecture of the processor (chip) is determined. ~~next~~

→ In floorplan stage we decide placement of different components and interconnect on the chip.

→ We develop a finite state machine consisting of different states and transition to explain the functionality of the chip.)

→ Depending upon the state machine we will design the ALU unit and register unit which are functional modules of a processor.

→ In the next step, these modules are placed on a chip surface using a computer aided design (CAD) software.

→ Each module description is defined using behavioral model with the help of either a hardware description language such as VHDL, PHDL or Verilog or by designing layout of ALU module in transistor level.

→ Next we design the logic gate module using (Leaf cell).

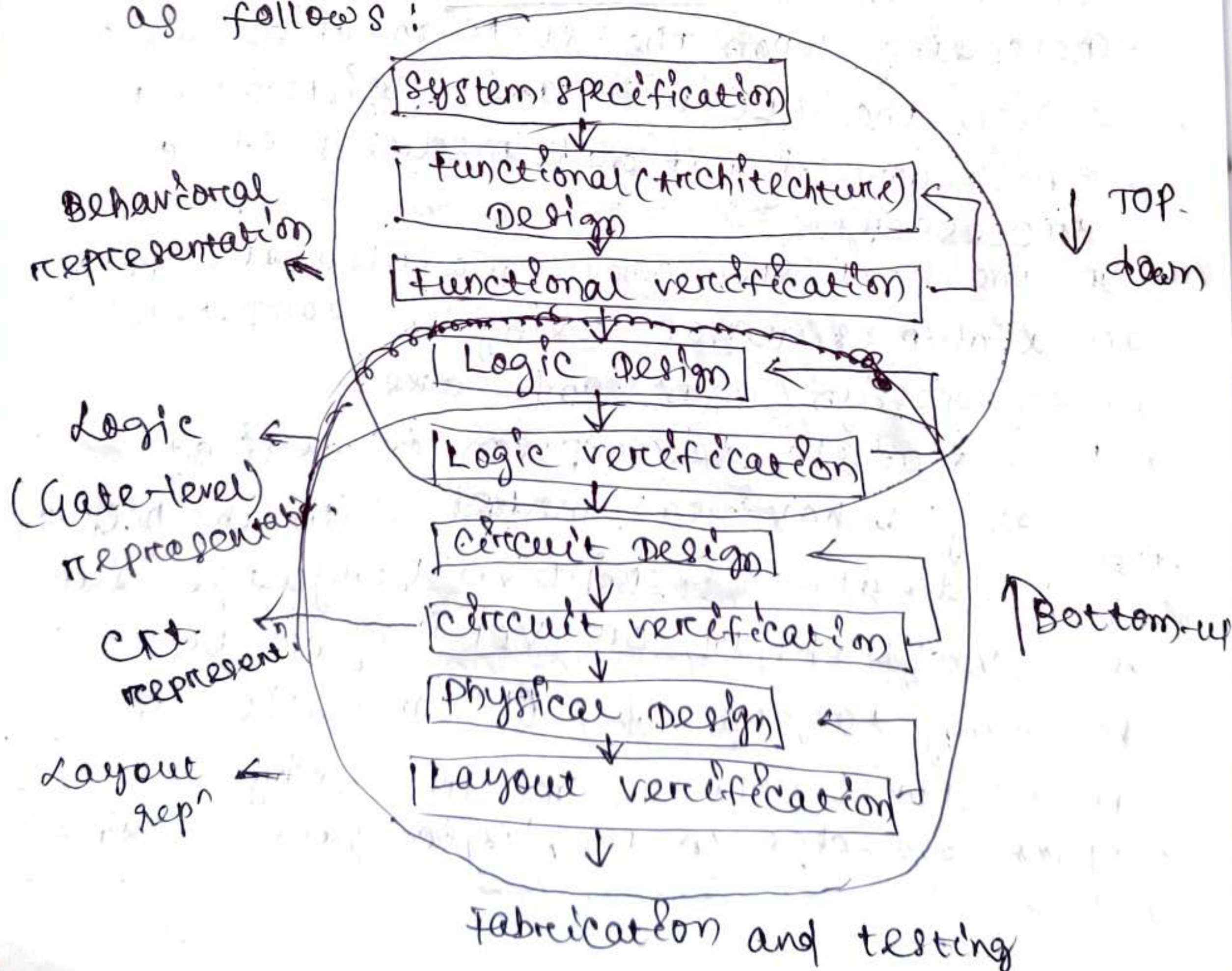
→ The leaf cells can be designed using some standard cells (NAND or NOR gate).

→ Every module can be designed by using its boolean expression.

→ Then we go to transistor level design as all gates consist of transistor (P-MOSFET and N-MOSFET).

→ Finally, mask is designed using CAD software and exported to foundry in the form of a specific file format (GDS - Geometric Design Specificatⁿ) for necessary fabrication of the chip.

→ A more precise design flow can be represented as follows :

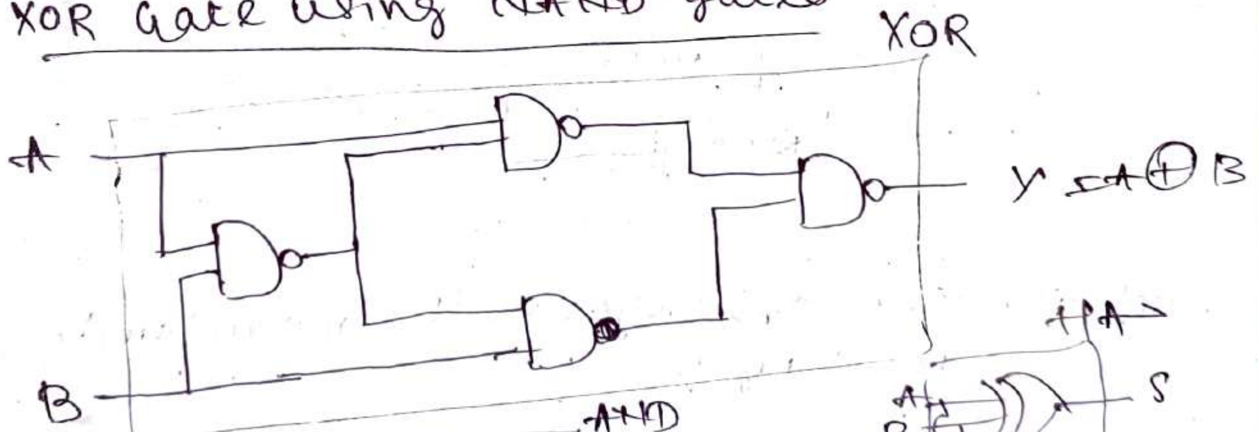


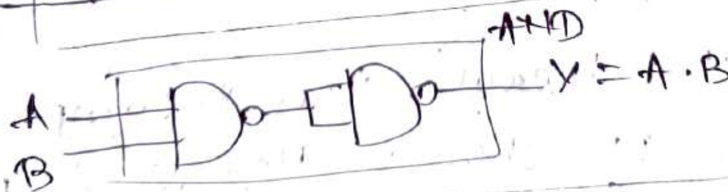
Bottom-up	Top-down
(i) This design starts from layout and ends with logic verification. (ii) This is also called as back-end design. eg. CADENCE	(i) The design starts with specification and ends at logic verification (ii) This is also called as front-end design. eg. vivado (Xilinx → AMD)

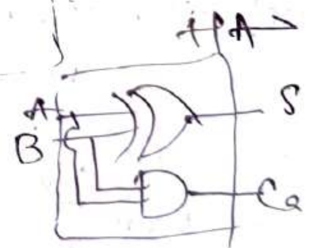
Design Hierarchy :-

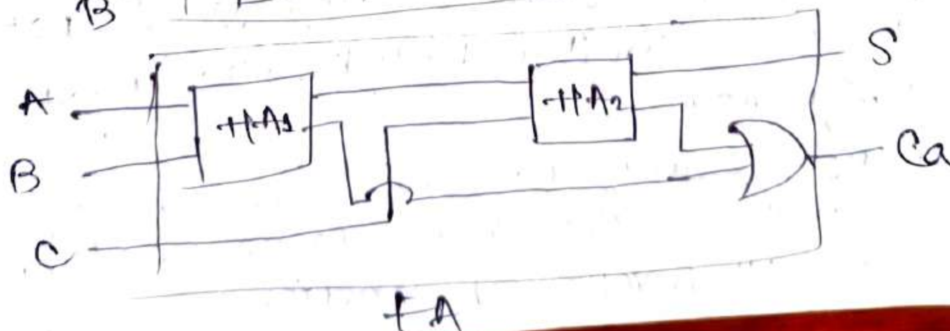
→ This technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

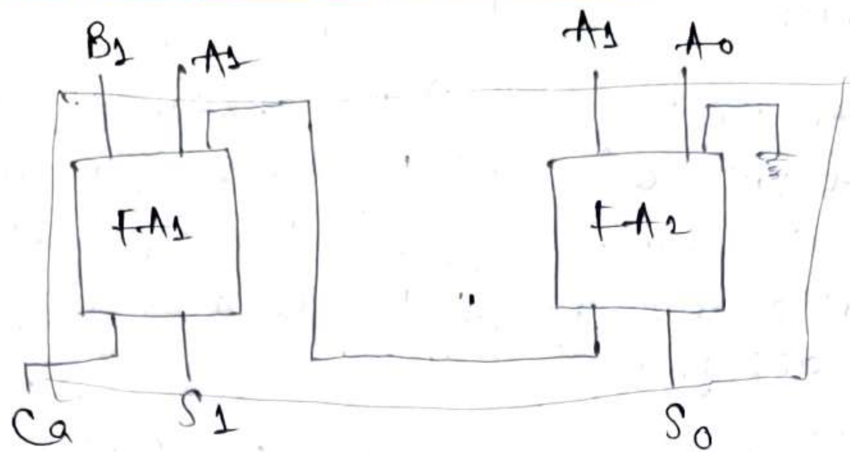
XOR Gate using NAND gates



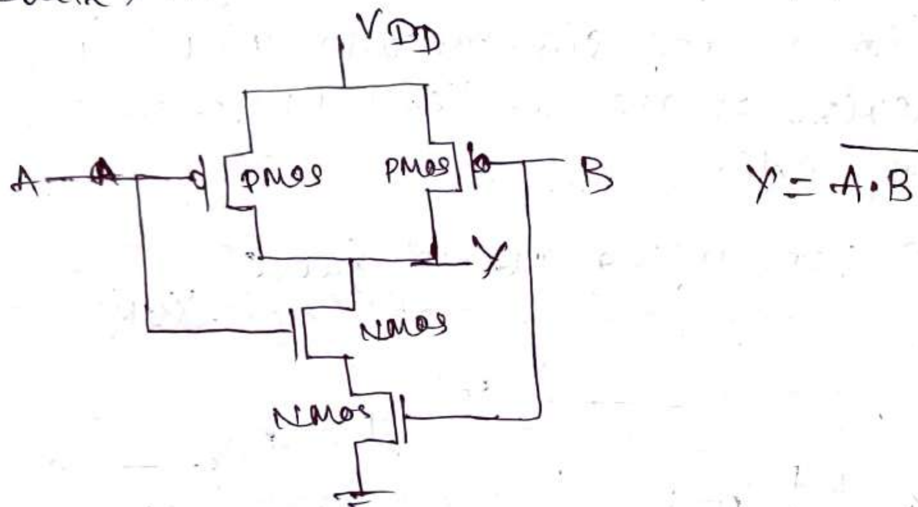








→ The example can be dividing adder circuit into full adder block, FA blocks into HA blocks/module, HA module into XOR & AND module, then XOR & AND module into NAND module, NAND module to transistor level.



concept of regularity, modularity and locality :-

Regularity :- The hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible.

→ Regularity usually reduces the no. of different modules that need to be designed and verified, at all levels of abstraction.

Modularity :- The various functional blocks which make up the larger system must have well-defined functions and interfaces.

Locality :- Internal details remain at the local level.

→ The concept of locality also ensures that connections are mostly between neighbouring modules, avoiding long-distance connections as much as possible.

VLSI Design styles :-

Field Programmable Gate Array (FPGA) :- (imp)

→ This is a hardware consisting of an array of gates which can be program by using hardware description language.

→ The no. of gates can be 20,000-25,000 or even more.

→ This design style provides a mean for ~~fast~~ prototyping and also for cost effective chip design especially for low volume applications.

→ It consist of ① I/O Buffers

② Configurable logic blocks (CLB)

③ Programmable interconnect structures.

→ The I/O buffers help in receiving and transmitting signal between FPGA and peripheral devices.

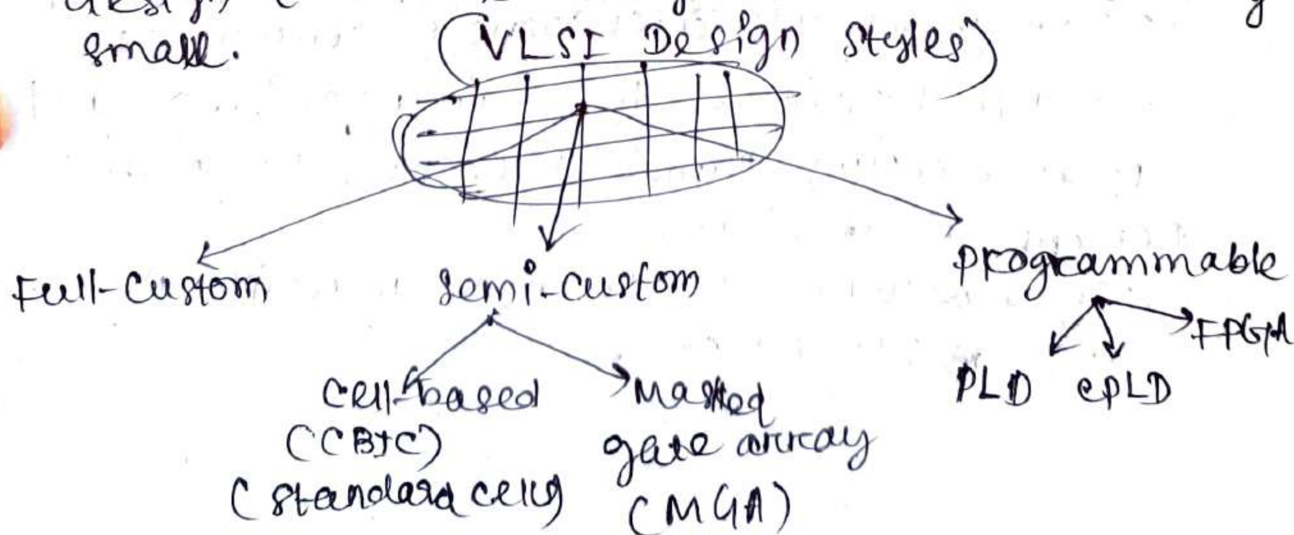
→ The CLB consists of multiple D-flipflops and 2:1 MUXes.

1. a 4-input combinational function generates memory look-up tables)
2. clock signal terminal
3. user-programmable multiplexers
4. two flip-flops

→ The programmable interconnects helps in signal routing between the CLB's and I/O buffers. This is accomplished by configuring the switch matrices.
(PSM - programmable switch matrices)

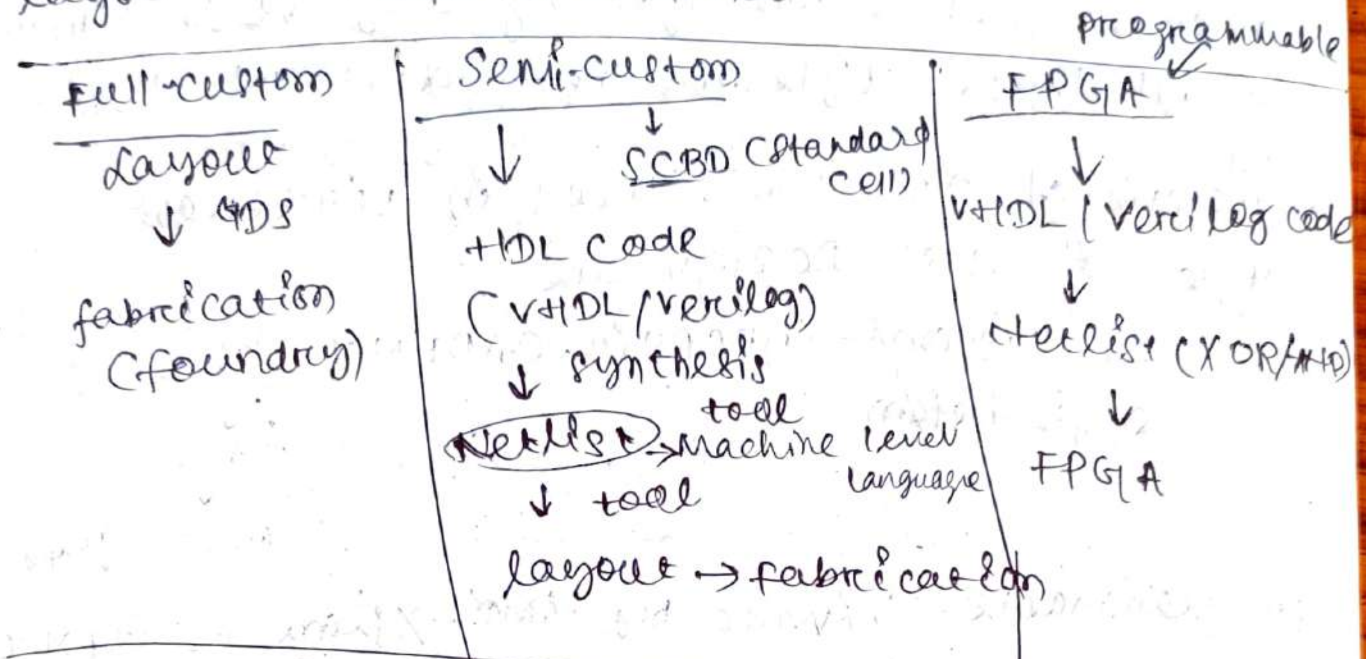
→ The PSM block is having 6 pass transistors.
→ The pass transistors can made on depending on the logic and behave like switch.
→ The complexity of FPGA is determined by the no. of CLB it contains.
→ A typical design flow in FPGA

→ FPGA have very short turn around time. i.e. the time required from start of design to availability in market is very small.



Full custom :-

→ In this design style we start from designing layout of transistor level.



→ In semi-custom design we start from writing HDL code.

→ A software tool converts this into corresponding netlist by the process synthesis, corresponding layout is generated next through standard cell based design process after optimization in interconnection it is send to foundry for fabrication.

→ But in programmable device flow, 1st HDL code is written, it is converted into corresponding netlist then downloaded into readymade hardware like FPGA, CPLD or PLD.

→ CPLD – Complex programmable Logic Device.

CAD Technology :- (Computer Aided Design)

→ There is always a help of software tool necessary for designing any VLSI circuit in all three styles. ~~we need different types~~

→ Example of CAD tools used in different styles of VLSI Design are

Full custom/ semi-custom — Synopsis, CADENCE, Siemens (only F.C)
↓
Tanner
↓
Mentor graph

Programmable - Vivado by AMD-Xilinx, CADENCE

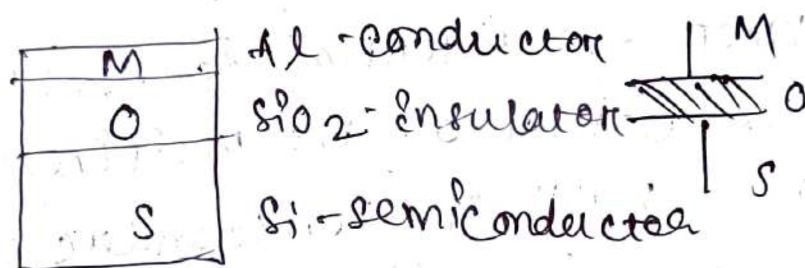
(FPGA → Basys
PYNQ,
ZYNQ
KRIA KV60

Chapter-3 MOS Transistor

The MOS structure, the MOS system under external bias, structure and operation of MOS transistor, MOSFET current-voltage characteristics, MOSFET scaling & small geometry effect, MOSFET capacitance.

MOS structure :-

→ It consist of metal and semiconductor separated by one insulator generally oxide.
→ Metal is generally aluminium (Al), insulator is silicon dioxide (SiO_2) and semiconductor is (Si) silicon.
→ As metal and SC are separated by an insulator it behaves as a capacitor and the structure looks like as follows:



→ The metal terminal is called Gate (G).
→ The SC terminal is called body or substrate (B/SS).

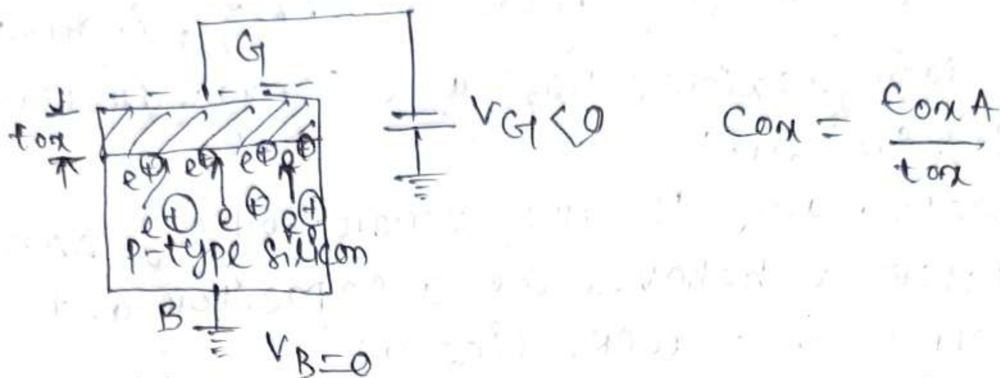
MOS system under external bias :-

→ The operation of MOS system can be understood by applying external bias (voltage).
→ Generally, the body terminal is connected to ground or zero potential.
→ The gate is supplied with -ve or +ve potential.
→ In our case we will consider the SC as p-type i.e. doped with trivalent acceptor atoms with concentration (N_A).

N_A = conc. of trivalent acceptor in cm^{-3}
V_G = potential or voltage applied to gate terminal.
V_B = potential applied to body terminal.

Operation of MOS capacitor :-

(i) When $V_G < 0$, $V_B = 0$ (Accumulation) :-

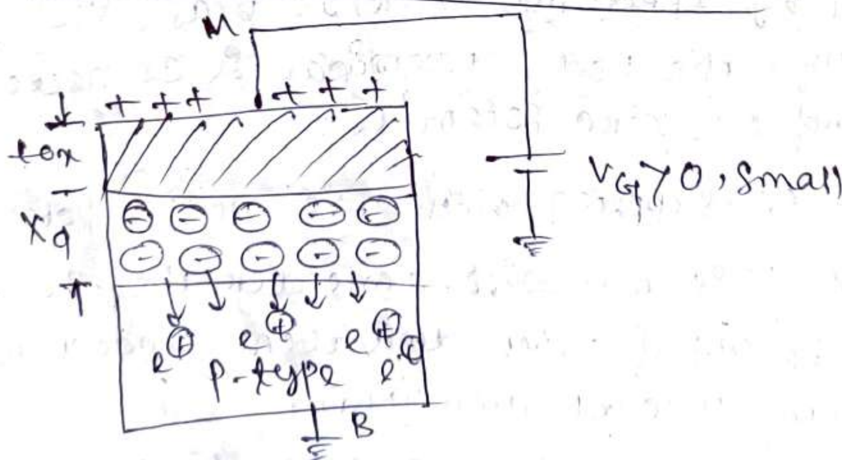


$$C_{ox} = \frac{\epsilon_{ox} A}{t_{ox}}$$

→ When -ve potential is applied to gate it will attract all the positively charged holes from bulk of semiconductor to its surface.

→ As, there is an accumulation of holes at the surface this mode of operation is called as accumulation and the surface is more p-type than the bulk.

(ii) When $V_G > 0$, but small, $V_B = 0$ (Depletion) :-



→ When the gate is supplied with +ve potential +ve charges are developed on the gate, this will repel holes from surface of semiconductor towards bulk by creating

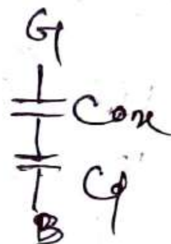
-vely charged anions.

→ The anions don't carry electricity and behaves an insulator.

→ ~~~~ As, there is depletion of free charge carriers at the surface of semiconductor, this mode of operation is called depletion.

→ There are 2 capacitors form across MOS system. One is due to oxide layer (C_{ox}) and the other one is due to depletion layer having thickness 'x_d' and capacitance C_d.

→ Hence, the equivalent capacitance can be represented as



$$\boxed{C_{eq} = \frac{C_{ox} \cdot C_d}{C_{ox} + C_d}}$$

where, $C_d = \frac{\epsilon_{si} A}{x_d}$, $\boxed{C_{eq} < C_{ox}}$

$$\boxed{x_d = \sqrt{\frac{2\epsilon_{si} |\phi_s - \phi_f|}{q N_A}}}$$

ϵ_{si} = Electrical permittivity of Si
$= 11.2 \times \epsilon_0 = 11.2 \times 8.854 \times 10^{-14}$ F/cm

ϕ_s = surface potential

ϕ_f = ~~~~ Bulk fermi potential

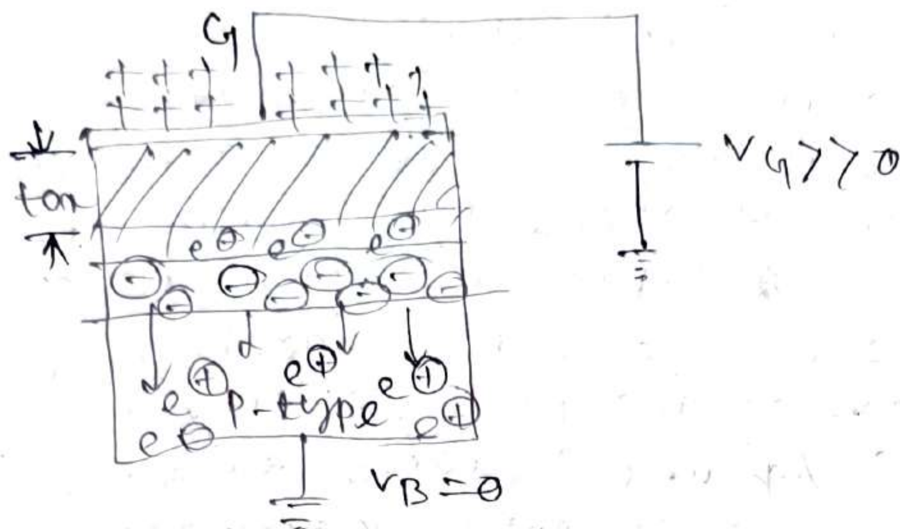
q = charge of $e^{\ominus} = 1.6 \times 10^{-19}$ C

$\phi_{fp} = \frac{KT}{q} \ln \frac{n_i}{N_a}$

or $\phi_{fn} = \frac{KT}{q} \ln \frac{N_d}{n_i}$

n_i = intrinsic carrier conc^n
$= 1.5 \times 10^{10}$ cm^{-3}

(iii) When $V_G >> 0$; $V_B = 0$ (Inversion) :-



→ As gate voltage becomes more +ve, all the holes from surface are repelled and go to bulk of substrate.

→ The depletion layer width become maximum denoted by 'X_{dm}' and represented by

$$X_{dm} = \sqrt{\frac{2\epsilon_{si}(2\phi_F)}{qN_A}}$$ and the depletion

layer charge can be defined by,

$$Q_0 = -qN_A X_d = -\sqrt{2qN_A \epsilon_{si}|-2\phi_F|}.$$

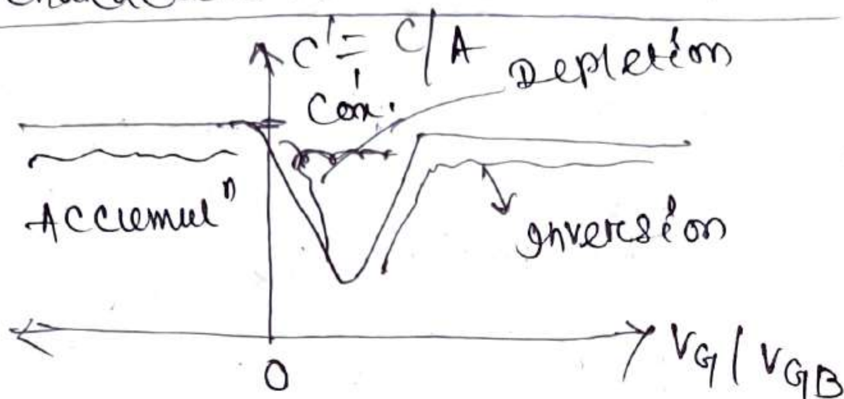
→ upon further increasing gate voltage electrons from bulk are attracted toward surface and accumulate there as shown in figure.

→ As the substrate is p-type and surface is behaving like N-type, this mode of operation is called as inversion.

→ The capacitance during this mode is represented by C_{ox} given by

$$C_{ox} = \frac{\epsilon_{ox} A}{t_{ox}}$$

CV characteristics of MOS capacitor :-



$$C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}} = \frac{C_{ox}}{A}$$

→ At the surface of substrate we get a layer of electron.

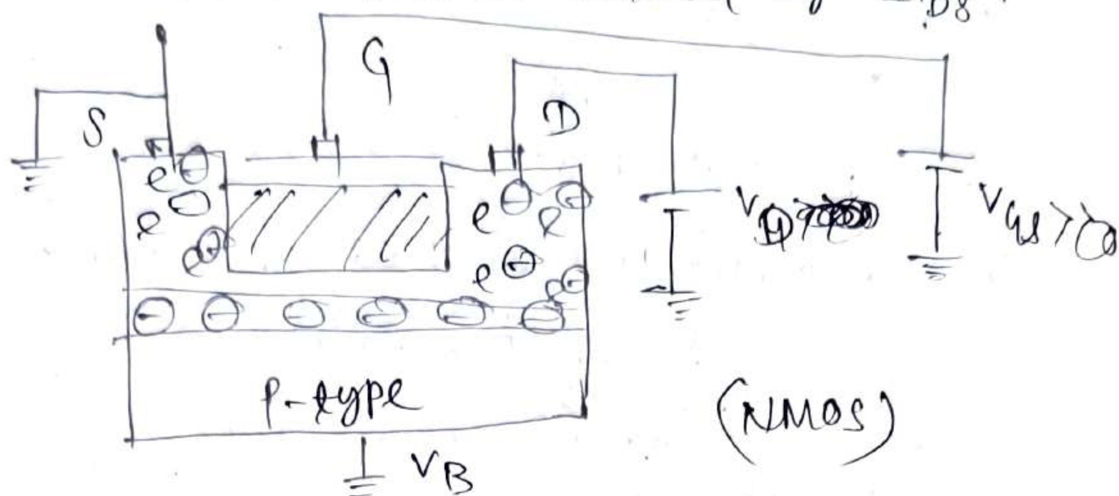
→ On both sides of the layer if we doped with heavy donor atoms source and drain regions are formed.

→ The terminal connected to ground is called source(S) and the terminal connected to supply voltage is called drain (D).

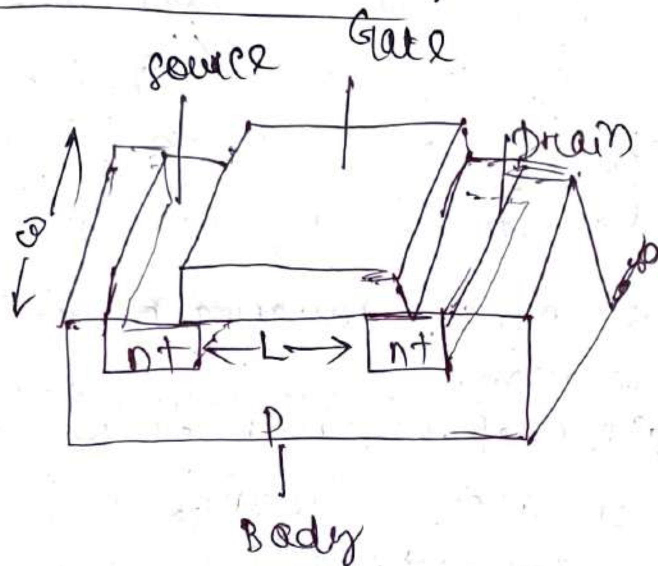
→ Hence, D and S terminals are interconvertable depending upon connected power supply.

→ When positive potential applied at drain $e^{\ominus}s$ from source move towards drain through channel created at the surface of substrate.

→ This forms a current whose direction is from drain to source denoted by I_{DS}.



Structure of MOSFET :- (3D)

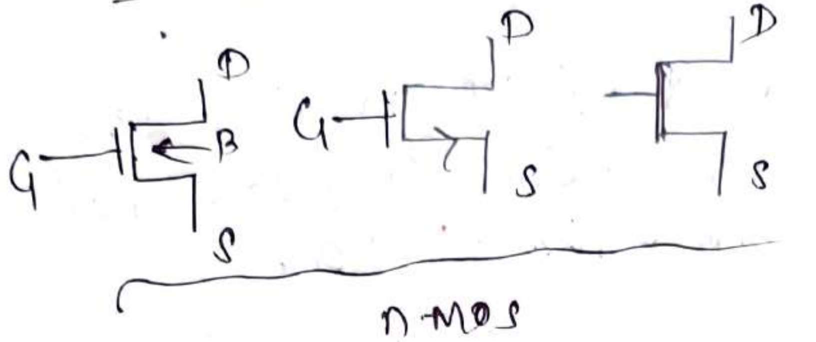


→ In P-type substrate channel consist of electrons and the MOSFET is of N type denoted by NMOS.

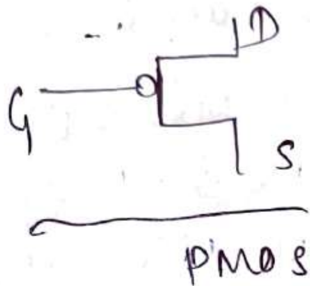
→ If the substrate is N-type MOSFET is P type and denoted by PMOS.

→ In NMOS channel is formed by applying +ve gate voltage where as in PMOS channel is formed by applying negative gate voltage.

Symbols used)



n-MOS



PMOS

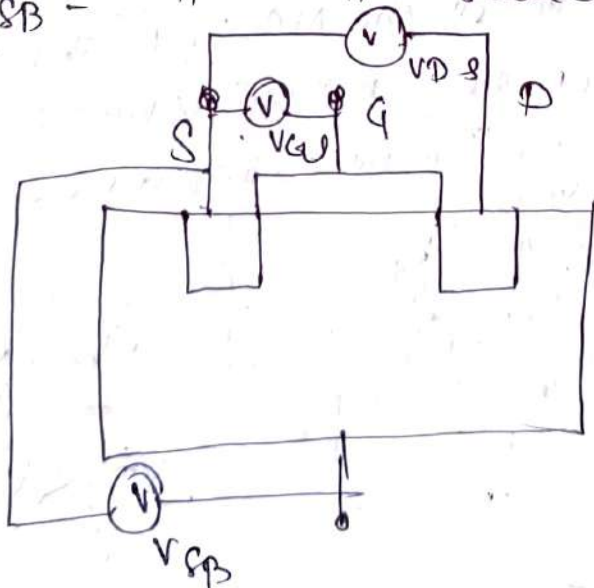
Operation of nMOS :-

→ There are three voltage parameters that can be used to control the operation of MOSFET.

V_{GS} - voltage betⁿ Gate & source $= V_G - V_S$

V_{DS} - " " drain & source $= V_D - V_S$

V_{SB} - " " source & body $= V_S - V_B$



→ In nMOS, source is connected to ground, but in pMOS, source is connected to highest available potential (+5V for eg.)

→ Generally body terminal is also connected to ground, to make $V_{SB} = 0$.

Case-1 $V_{GS} < V_T$, V_{DS} = Any value

V_T = Threshold voltage of MOSFET.

→ It is the minimum gate voltage required to form the channel at the surface of substrate.

→ For this course we will assume,

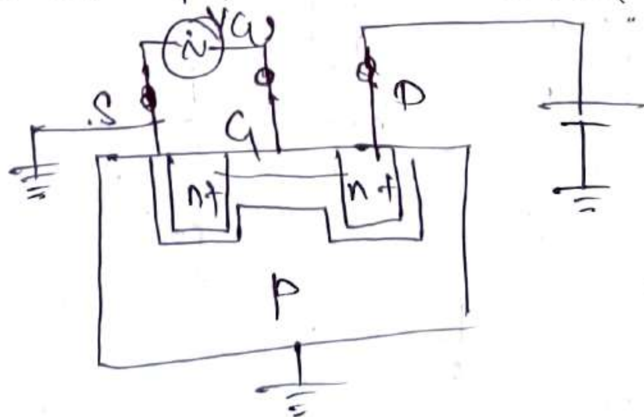
$V_{Tn} = V_T$ for NMOS (1 V) and

V_{Tp} = for nMOS = −1 V.

→ When $V_{GS} < V_T$ there is no channel formed at surface of substrate. hence, no electrons flows from source to drain. so, no current flows across the MOSFET and the device is in cut-off mode (device is off).

→ The mode of operation is called as cut-off.

Case-2



$V_{GS} > V_{Tn}$

$V_{DS} < V_{GS} - V_{Tn}$

let $V_{GS} = 3V$

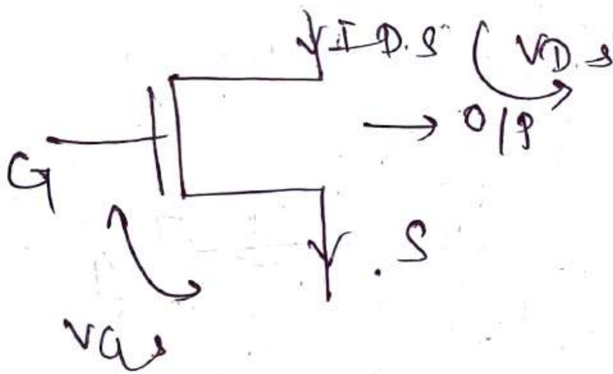
$V_{GS} - V_{TN} = 3 - 1 = 2V$

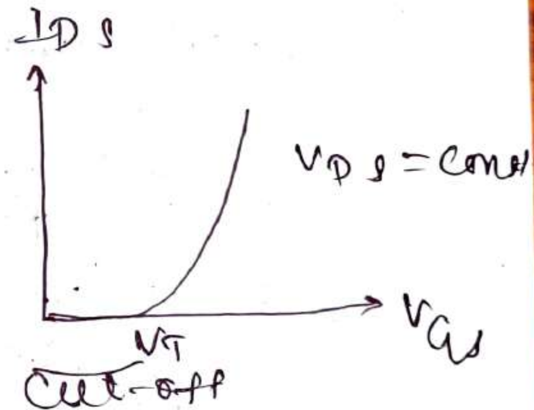
→ V_{GS} is fixed

→ V_{DS} is increasing from 0 to $V_{GS} - V_{TN}$ (2V)

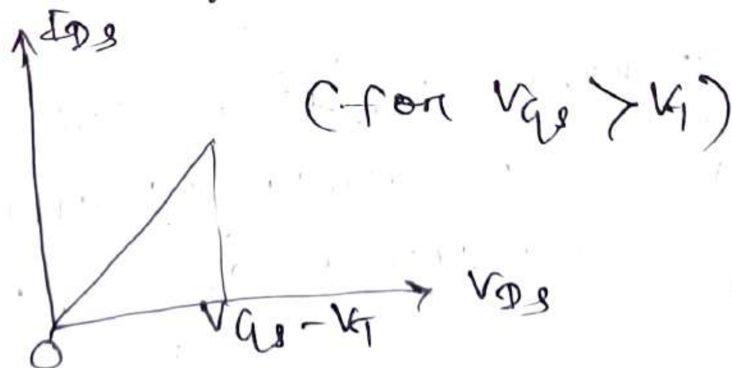
→ As V_{DS} increasing, it will attract electrons from source towards drain and current will increase linearly.

→ So, the transfer characteristics between input voltage (V_{GS}) and output current (I_{DS}) can be be represented as follows.





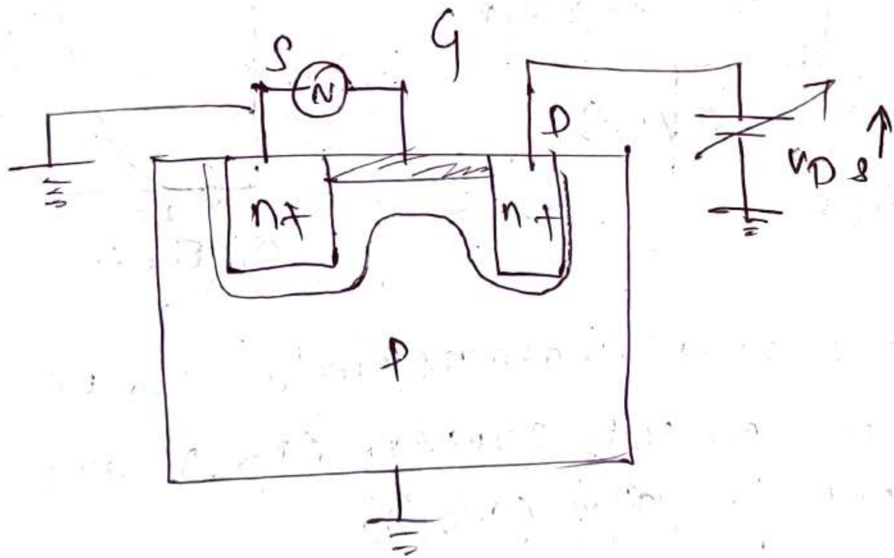
→ The output characteristics can be drawn between output current (I_{DS}) and output voltage (V_{DS}).



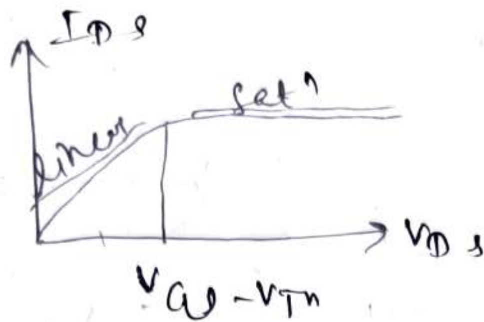
→ As the current increases linearly, this mode of operation is called as linear mode of operation.

Case-3 $V_{GS} > V_{TN}$ $V_{DS} \geq V_{GS} - V_{TN}$

→ Beyond $V_{GS} - V_{TN}$, if V_{DS} increased at the drain terminal the reverse biasness of drain to substrate pn junction increases which in turn increases the depletion region width. This decreases channel width at the drain side, as shown in fig. Hence, the current doesn't increase and remain constant.



→ As the current remains constant and its saturated, the mode of operation is called saturation mode.



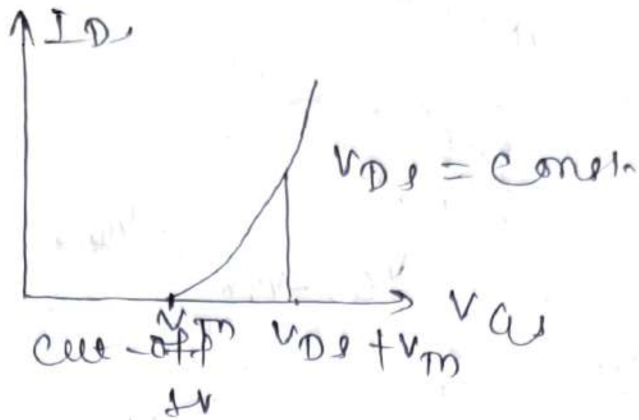
N-MOS

voltage	mode of operation	Device
$V_{GS} < V_{Tn}$	cut-off, $I_D = 0$	off
$V_{GS} > V_{Tn}$, $V_{DS} < V_{GS} - V_{Tn}$	linear $I_D \neq 0$	on
$V_{GS} > V_{Tn}$, $V_{DS} \geq V_{GS} - V_{Tn}$	saturation $I_D \neq 0$	on

P-MOS

voltage	mode of operation	Device
$V_{GS} > V_{Tp}$	cut-off, $I_D = 0$	off
$V_{GS} \leq V_{Tp}$, $V_{DS} \geq V_{GS} - V_{Tp}$	linear, $I_D \neq 0$	on
$V_{GS} \leq V_{Tp}$, $V_{DS} \leq V_{GS} - V_{Tp}$	saturation, $I_D \neq 0$	on

For n-MOS



For saturation mode

$$V_{DS} \geq V_{GS} - V_{Tn}$$

$$V_{DS} = V_{GS} - V_{Tn}$$

$$V_{GS} \leq V_{DS} + V_{Tn}$$

Let, $V_{Tn} = 1\ V$, $V_{DS} = 5V$

$V_{GS} = 0$ to $5V$

for cut-off

$$V_{GS} < V_{Tn}$$

$$0 < 1\ V \checkmark$$

$$V_{GS} \geq V_{Tn}$$

Two condition

$V_{GS} = V_{Tn}$ (saturation)

$V_{GS} > V_{Tn}$ (linear)

$V_{GS} = V_{Tn}$ $(V_{GS} = 1)$ $V_{GS} \geq V_T$

$$V_{DS} \geq V_{GS} - V_T$$

$$5 > 0 \checkmark$$

for linear $V_{GS} \leq V_{TN}$,

$V_{DS} < V_{GS} - V_T$

$5 < V_{GS} - V_T$

$5 < V_{GS} - 1$

$V_{DS} = 5V$
$V_{TN} = 1V$

$V_{DS} + V_T < V_{GS}$, $6 < V_{linear}$ (Linear condⁿ)

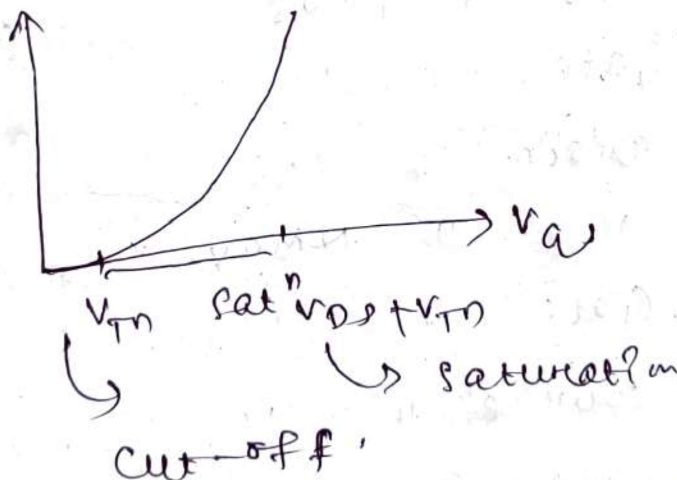
output characteristics / transfer characteristics

I_D = constant V_{DS}.

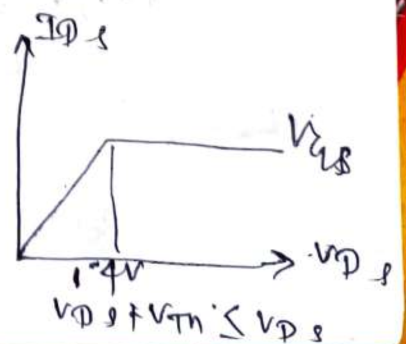
when $V_{GS} < V_{TN}$; cut-off

$V_{GS} \geq V_{TN}$, $V_{GS} \leq V_{DS} + V_{TN}$, saturation

$V_{GS} > V_{TN}$ $V_{GS} \geq V_{GS} + V_{TN}$



output characteristics



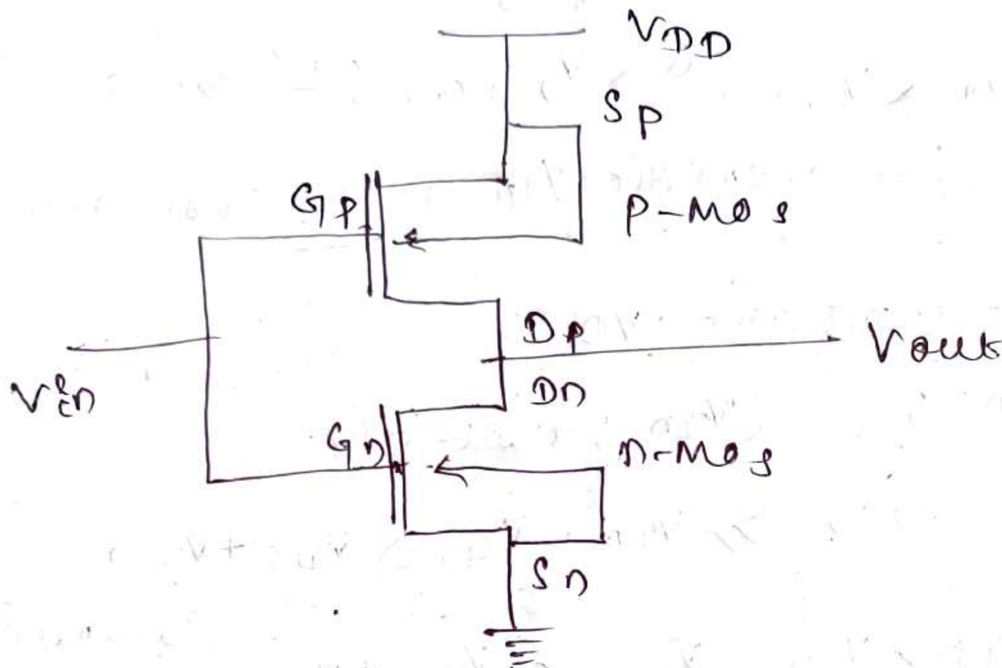
for linear $V_{DS} < V_{GS} - V_{TN}$

satⁿ, $V_{DS} \geq V_{GS} - V_{TN}$

Let, $V_{GS} = 5V$

C-MOS inverter operation :-

A C-MOS inverter consist of one P-MOS and one n-MOS connected as shown in figure.



Sp = source of pMOS

Gp = Gate " "

Dp = Drain " "

Dn = " " NMOS

Gn = Gate " "

Sn = source " "

VDD = 5V (let)

Case-1

$v_{in} = '0'$

$v_{in} = 0V$

$v_{Gp} = 0V$

$v_{Gn} = 0V$

Logic 0 = 0V

logic 1 = 5V

PMOS

$V_{GS} < V_{TP}$

$V_{Gp} - V_{Sp} < V_{TP}$

$0V - 5V < -1V$

$\Rightarrow -5V < -1V$ (✓)

∴ PMOS is ON & PMOS is short.

NMOS $V_{GS} > V_T$

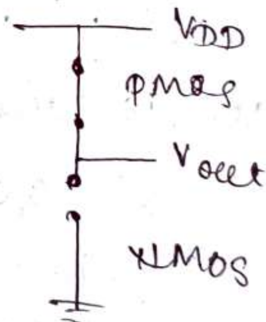
$V_{Gn} - V_{Sn} > V_{Tn}$

$0 - 0 > 1.$

$0 > 1$ (✗)

∴ NMOS is off and NMOS is open.

$\Rightarrow v_{out} = v_{DD} =$ Logic 1



Case-2

$v_{in} = '1'$

$v_{in} = 5V$

$v_{GP} = 5V$

$v_{Gn} = 5V$

PMOS

$V_{GS} < V_{TP}$

$\Rightarrow V_{GP} - V_{SP} < V_{TP}$

$\Rightarrow 5 - 5 < -1$

$\Rightarrow 0 < -1$ (✗)

∴ PMOS is off

⇒ PMOS is open.

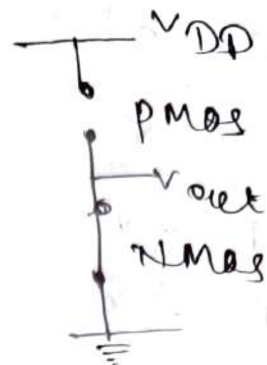
NMOS

$V_{GS} > V_{TN}$

$\Rightarrow V_{GN} - V_{SN} > V_{TN}$

$\Rightarrow 5 - 0 > 1$

$\Rightarrow 5 > 1$ (✓)



∴ NMOS is ON. $\Rightarrow V_{out} = 0V =$ logic 0

⇒ NMOS is short.

V_{in}	PMOS	NMOS	V_{out}
logic 0 0V	ON Short	off open	logic 1 5V
logic 1 5V	off open	ON short	logic 0 0V

MOSFET Threshold voltage :-

→ Threshold voltage of MOSFET has 4 component.

(i) Gate to substrate work function difference (ϕ_{GC})

(ii) voltage equivalent to potential required for surface inversion ($-2\phi_F$)

(iii) voltage equivalent to compensate immobile acceptor ions present below the channel represented by $Q_B = -\sqrt{2qN_A\epsilon_{si}|-2\phi_F + V_{SB}|}$

$V_{SB} = V_S - V_B$ (source, Body)

for $V_{SB} = 0$, $Q = Q_0$

$$Q_{B0} = -\sqrt{2qN_a\epsilon_{Si}|-2\phi_F|}$$

$$V = \frac{Q}{C} = \frac{Q_{B0}}{C_{ox}}$$

(iv) The last component is equivalent to unintensional charges developed inside the oxide during fabrication.

→ This potential is represented by $\frac{Q_{ox}}{C_{ox}} = V_{ox}$

∴ Hence, threeshold voltage expression can be expressed as,

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad \text{—(1)}$$

for, $V_{SB} = 0$, $V_T = V_{T0}$

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad \text{—(2)}$$

Subtracting eqⁿ (2) from (1),

$$V_T - V_{T0} = -\frac{Q_B}{C_{ox}} + \frac{Q_{B0}}{C_{ox}}$$

$$\Rightarrow V_T = V_{T0} - \frac{Q_B}{C_{ox}} + \frac{Q_{B0}}{C_{ox}}$$

$$\Rightarrow V_T = V_{T0} - \left(\frac{Q_B - Q_{B0}}{C_{ox}}\right) \quad \text{—(3)}$$

$$\Rightarrow \frac{Q_B - Q_{B0}}{C_{ox}} = \frac{-\sqrt{2qN_a\epsilon_{Si}|-2\phi_F + V_{SB}|} + \sqrt{2qN_a\epsilon_{Si}|-2\phi_F|}}{C_{ox}}$$

$$= \frac{-\sqrt{2qN_a\epsilon_{Si}}\left[\sqrt{|-2\phi_F+V_{SB}|}-\sqrt{|-2\phi_F|}\right]}{C_{ox}}$$

$$\Rightarrow \frac{Q_B - Q_{B0}}{C_{ox}} = -\gamma\left(\sqrt{|-2\phi_F+V_{SB}|}-\sqrt{|-2\phi_F|}\right) \quad \text{--- (4)}$$

Put eq^n (4) in (3)

$$\Rightarrow \boxed{V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F+V_{SB}|}-\sqrt{|-2\phi_F|}\right)} \quad \text{--- (5)}$$

at $V_{SB} = 0$,

$$V_T = V_{T0}$$

→ Here, γ is called as substrate-bias effect or (body effect) coefficient.

→ When substrate is given some potential instead of connecting to the ground it effects the threshold voltage of the device and this effect is called as body effect.

parameter	nMOS	pMOS
ϕ_F	−	+
Q_B, Q_{B0}	−	+
γ	+	−
V_{SB}	+	−

$$V_{Tn0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$V_{Tp0} = \Phi_{GC} + 2\phi_F + \frac{\Phi_{B0}}{C_{ox}} + \frac{\Phi_{ox}}{C_{ox}}$$

$$V_{Tp} = V_{Tp0} - \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

$$V_{Tn} = V_{Tn0} + \gamma\left(\sqrt{-2\phi_F + V_{SB}} - \sqrt{|-2\phi_F|}\right)$$

Q. Calculate the threshold voltage V_{T0} at $V_B = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}\ cm^{-3}$, polysilicon gate doping density $N_D = 2 \times 10^{20}\ cm^{-3}$, gate oxide thickness $t_{ox} = 500\ Å$ and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}\ cm^{-2}$.

(5)

Note — For polysilicon gate

It is a special type of silicon material which can be doped to obtain desired work function.

→ For n-type polysilicon $\Phi_G = 0.55\ eV$.

→ For p-type polysilicon $\Phi_G = 1.1 + 0.55 = 1.65\ eV$.

Sol:

$$\phi_{FS} = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right)$$
(substrate)

$$= 0.0259 \ln\left(\frac{1.5 \times 10^{10}}{10^{16}}\right)$$

$$= -0.35\ V$$

$$\phi_{GC} = \phi_S - \phi_G = -0.35V - 0.55V$$
$$= -0.9V$$

$$\therefore V_T = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$Q_{B0} = -\sqrt{2qN_a\epsilon_{si}|-2\phi_F|}$$
$$= -\sqrt{2 \times 1.6 \times 10^{-19} \times 10^{16} \times 11.7 \times 8.854 \times 10^{-14} |-2 \times 0.35|}$$
$$= -4.82 \times 10^{-8} \ C/cm^2$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97 \times 8.85 \times 10^{-14}}{500 \times 10^{-8}}$$
$$= 7.03 \times 10^{-8} \ F/cm^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-4.82 \times 10^{-8}}{7.03 \times 10^{-8}} = -0.685 \ C/F$$

$$Q_{ox} = q \cdot N_{ox}$$
$$= 1.6 \times 10^{-19} \times 4 \times 10^{10}$$

$$\Rightarrow \frac{Q_{ox}}{C_{ox}} = 0.09$$

$$\therefore V_T = -0.9 + 2 \times 0.35 + 0.685 - 0.09 = 0.395 \ V.$$

Q. Consider the following p-channel MOSFET process. Substrate doping $N_D = 10^{15}\ cm^{-3}$, polysilicon gate doping density $N_D = 10^{20}\ cm^{-3}$, gate oxide thickness $t_{ox} = 650 Å$, and oxide-interface charge density $N_{ox} = 2 \times 10^{10}\ cm^{-2}$. Use $\epsilon_{si} = 11.7\epsilon_0$ and $\epsilon_{ox} = 3.97\epsilon_0$ for the dielectric coefficients of silicon and silicon-dioxide resp.

Calculate the threshold voltage V_{TO} for $V_{SB} = 0$.

Sol^n $\phi_{F\,substrate} = \frac{KT}{q} \ln \frac{N_d}{n_i}$

$$= 0.0259 \ln\left(\frac{10^{15}}{1.45 \times 10^{10}}\right)$$

$$= 0.2886\ V$$

$$\phi_{GC} = \phi_S - \phi_G = 0.2886 - 1.65 = -1.36\ V$$

$$Q_{B0} = -\sqrt{2qN_a\epsilon_{si}|-2\phi_F|}$$

$N_A N_D = n_i^2$

$N_A = \frac{n_i^2}{N_D} = 225 \times 10^3$

$$= -\sqrt{2 \times 1.6 \times 10^{-19} \times 225 \times 10^3 \times 11.7 \times 8.854 \times 10^{-14}\ |-2 \times 0.2886|}$$

$$= -2.074 \times 10^{-13}\ C/cm^2$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97 \times 8.854 \times 10^{-14}}{650 \times 10^{-8}}$$

$$= 5.41 \times 10^{-8}\ F/cm^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-2.074 \times 10^{-13}}{5.41 \times 10^{-8}} = 3.833 \times 10^{-6}\ C/F$$

$$Q_{ox} = q \cdot N_{ox} = 1.6 \times 10^{-19} \times 2 \times 10^{10}$$

$$= 3.2 \times 10^{-9}$$

$$\Rightarrow \frac{Q_{ox}}{C_{ox}} = \frac{3.2 \times 10^{-9}}{5.41 \times 10^{-8}} = 0.06\ C/F$$

$\times 10^{-14}$

$= 0.395$ V.

$$\therefore V_T = \phi_{GC} + 2\phi_F + \frac{Q_{Bo}}{C_{ox}} + \frac{Q_{ox}}{C_{ox}}$$

$$= -1.36 + 2 \times 0.2886 + 3.833 \times 10^{-6} + 0.06$$

$$= -0.72279 \text{ V}$$

0.5772

MOSFET current-voltage characteristics :-

Gradual channel Approximation :-

.06

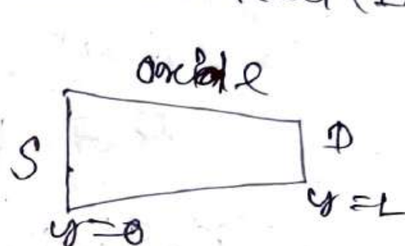
→ As per this approximation the current flows in channel only due to horizontal motion of electrons as the channel thickness is very small.

Assumption :

→ $V_{SB} = 0$

→ V_{T0} is constant along the entire channel.

→ Horizontal electric field (E_y) dominates vertical electric field (E_x).



→ Let us assume,

the device in linear mode.

Let, $V_c(y)$ = channel voltage with respect to the source at position y.

L = Length of channel

Boundary conditions:-

$$V_c(y=0) = V_S = 0$$

$$V_c(y=L) = V_{DS}$$

Let $Q_i(y)$ = the mobile electron charge density inside channel at any point of y

$$Q_i(y) = -C_{ox}\left[V_{GC} - V_c(y) - V_{T0}\right]$$

→ The charge flowing in the channel is due to effective voltage $V_{GS} - V_{T0} - V_c(y)$.

Let us consider, an elemental channel region having length ('dy') and resistance 'dR'.

$$R = \rho l/A = \frac{1}{\sigma}\frac{l}{A}$$

dR is given by,

$$dR = -\frac{1}{\sigma}\frac{dy}{W \cdot x_d(y)}$$

$x_d(y)$ = Thickness of channel maximum at source and minimum at drain

$\sigma = q\mu_n N_a$, | Where, μ_n = mobility of $e^{\ominus}$ → Easiness with which $e^{\ominus}$ moves.

$$\Rightarrow dR = -\frac{dy}{q\mu_n N_a W x_d(y)}$$

$$\Rightarrow dR = \frac{-dy}{(W\mu_n)(qN_a x_d(y))}$$

$$= \frac{-dy}{W\mu_n Q_i(y)}$$

Where, $Q_i(y)$ = charge density

$$dV_c = I_D dR$$

$$\Rightarrow dV_c = I_D\left(\frac{-dy}{W\mu_n Q_i(y)}\right)$$

$$\Rightarrow dV_c = \frac{-I_D}{W\mu_n Q_i(y)} dy$$

$$\Rightarrow -I_D dy = W\mu_n Q_i(y) dV_c$$

$$\Rightarrow -\int_0^L I_D dy = \int W\mu_n \left(-C_{ox}(V_{GS} - V_c(y) - V_{T0})\right) dV_c$$

$$\Rightarrow \int_0^L I_D \, dy = \int_0^{V_{DS}} W \mu_n C_{ox} \left[V_{GS} - V_C(y) - V_{T0} \right] dV_C$$

$$\Rightarrow I_D L = W \mu_n C_{ox} \int_0^{V_{DS}} \left(V_{GS} - V_C(y) - V_{T0} \right) dV_C$$

$$= W \mu_n C_{ox} \left[\int_0^{V_{DS}} (V_{GS} - V_{T0}) \, dV_C - \int_0^{V_{DS}} V_C(y) \, dV_C \right]$$

$$\Rightarrow I_D L = W \mu_n C_{ox} \left(\left[(V_{GS} - V_{T0}) V_C \right]_0^{V_{DS}} - \left[\frac{V_C^2(y)}{2} \right]_0^{V_{DS}} \right)$$

$$= W \mu_n C_{ox} \left((V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\Rightarrow \boxed{ I_{D\,lin.} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(2 (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2 \right) }$$

→ For saturation mode of operation, the condition is $V_{DS} \geq V_{GS} - V_{T0}$.

putting $V_{DS} = V_{GS} - V_{T0}$ in linear mode drain current eqn.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2 (V_{GS} - V_{T0})(V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2 \right]$$

$$= \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(2 (V_{GS} - V_{T0})^2 - (V_{GS} - V_{T0})^2 \right)$$

$$\Rightarrow \boxed{ I_{D\,sat} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{T0})^2 }$$

$$\Rightarrow \int_0^L I_D\,dy = \int_0^{V_{DS}} W \mu_n C_{ox} [V_{GS} - V_C(y) - V_{T0}]\,dV_C$$

$$\Rightarrow I_D L = W \mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_C(y) - V_{T0})\,dV_C$$

$$= W \mu_n C_{ox} \left[\int_0^{V_{DS}} (V_{GS} - V_{T0})\,dV_C - \int_0^{V_{DS}} V_C(y)\,dV_C \right]$$

$$\Rightarrow I_D L = W \mu_n C_{ox} \left((V_{GS} - V_{T0}) V_C \Big]_0^{V_{DS}} - \frac{V_C^2(y)}{2} \Big]_0^{V_{DS}} \right)$$

~~$= W \mu_n C_{ox} [V_{GS} - V_T - V_C(y)] V_{DS}$~~

$$= W \mu_n C_{ox} \left((V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\Rightarrow \boxed{I_{D\,lin.} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(2 (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2 \right)}$$

→ For saturation mode of operation, the condition is $V_{DS} \geq V_{GS} - V_{T0}$.

putting $V_{DS} = V_{GS} - V_{T0}$ in linear mode drain current eqn.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2 (V_{GS} - V_{T0})(V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2 \right]$$

$$= \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2 (V_{GS} - V_{T0})^2 - (V_{GS} - V_{T0})^2 \right]$$

$$\Rightarrow \boxed{I_{D\,sat} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{T0})^2}$$

To simplify the eqⁿ, we define

$$K = K' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$$

$K' \rightarrow$ the process transconductance parameter

$K \rightarrow$ the device transconductance parameter

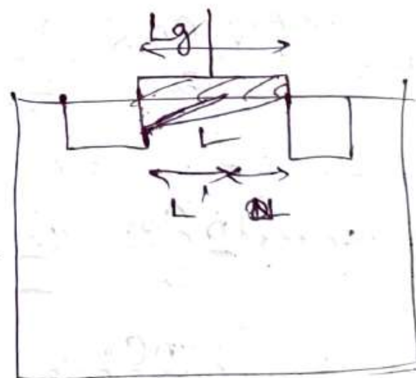
Channel length modulation :-

→ During saturation the current remain constant w.r.t. increase in V_{DS}.

→ However, when the device size is reduced the drain current in saturation doesn't remain constant and increases with V_{DS} due to shortening of channel length. This phenomenon is due to channel length modulation.

→ During saturation mode the channel length is reduced and the effective channel length is less than gate length as shown in figure.

→ During linear mode,



$$L = L_g$$

$$L = L' + \Delta L$$

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$$

&

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2} \frac{W}{L'} (V_{GS} - V_T)^2$$

$$\Rightarrow I_{D,sat} = \left(\frac{\mu_n C_{ox}}{2} W\right) \frac{1}{L'} (V_{GS} - V_{T0})^2 \quad \text{--- (1)}$$

$$\because \frac{1}{L'} = \frac{1}{L-\Delta L} = \frac{1}{L}\left(\frac{1}{1-\frac{\Delta L}{L}}\right)$$

$$= \frac{1}{L}\frac{1}{1-\lambda V_{DS}} \quad \left(\text{where, } \Delta L = L\lambda V_{DS}\right)$$

$$= \frac{1}{L}\left(\frac{1+\lambda V_{DS}}{(1-\lambda V_{DS})(1+\lambda V_{DS})}\right)$$

$$\Rightarrow \frac{1}{L'} = \frac{1}{L}\left(\frac{1+\lambda V_{DS}}{1^2 - \lambda^2 V_{DS}^2}\right) \quad (0<\lambda<1) \quad (\lambda^2 \simeq 0)$$

$$\Rightarrow \boxed{\frac{1}{L'} = \frac{1}{L}(1+\lambda V_{DS})} \longrightarrow (2)$$

putting eqⁿ (2) in (1),

$$\boxed{I_{D,sat} = \left(\frac{\mu_n C_{ox}}{2} W\right)\left(\frac{1}{L}\right)(1+\lambda V_{DS})(V_{GS}-V_{T0})^2} \longrightarrow (3)$$

→ Eqⁿ (3) represents actual drain current equation in saturation mode by considering channel length modulation effect.

Here, λ = channel length modulation coefficient

→ λ is a model parameter used to explain channel length modulation effect in saturation mode. $(\lambda < 0.1)$

Q. Find out the ratio of drain current at saturation mode to linear mode at $V_{DS} = 5V$, $V_{GS} = 1V$ and $V_T = 0.8V$. Given $\lambda = 0.1$.

Sol^n

$$\frac{I_{D,lin}}{I_{D\,sat}} = \frac{\frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2\right)}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2(1+\lambda V_{DS})}$$

$$= \frac{2(1-0.8)5-5^2}{(1-0.8)^2(1+0.1\times 5)}$$

$$= \frac{-23}{0.06} = -383.34$$

$$\Rightarrow \frac{I_{D\,sat}}{I_D} = -2.6\times 10^{-3}$$

$$K_n = \mu_n C_{ox}\frac{W}{L}$$

$$K_n' = \mu_n C_{ox}$$

$$\Rightarrow K_n = K_n'\frac{W}{L}$$

$K_n' = PPP$

Scalling in MOSFET :-

→ As VLSI industry demands more and more transistors to be accomodated in same space, decrease in transistor size is essential.

→ This scalling down process has many effects called as scalling effect.

→ There are two types of scalling.

(i) constant voltage scaling
(ii) constant field scalling

(i) constant voltage scalling :—

→ ~~The scalling of~~ the device
→ In this scalling method the dimension of the MOSFET are reduced by a factor of 'S'.
The power supply voltage and terminal voltages remain constant.

Quantity	before scaling	Quantity after scaling
w, l, t_{ox}		$w/S, l/S, t_{ox}/S$
voltage $= V_{DD}, V_T$		V_{DD}, V_T
Doping density, N_D, N_A $\left(N_D = \frac{\text{No. of dopant}}{\text{Area}}\right)$		$S^2 N_D, S^2 N_A$
current, I_D		$S.I_D$
oxide capacitance, C_{ox}		$S.C_{ox}$

$$I_D = \frac{\mu_n \epsilon_{ox}}{2 t_{ox}} \frac{w}{L} (V_{GS} - V_T)^2$$

$$I_D' = \frac{\mu_n \epsilon_{ox}}{2 t_{ox}'} \frac{w'}{L'} (V_{GS} - V_T)^2$$

$$\frac{I_D'}{I_D} = \frac{\frac{w'}{L' t_{ox}'}}{\frac{w}{L t_{ox}}} = \frac{\frac{w}{S}}{\frac{L}{S} \frac{t_{ox}}{S}} \times \frac{L t_{ox}}{w}$$

$$= S$$

Power dessipation, $P = I_{DS} V_{DS}$ — $P' = S.P$

Power density $= \frac{P}{A}$ — $\frac{P'}{A'} = \frac{SP}{\frac{W}{S} \cdot \frac{L}{S}}$

$= S^3 \left(\frac{P}{A}\right)$

→ Constant voltage scaling increases the drain current density and power density by a factor of S^3.

→ This causes serious reliability problem due to production of more heat and leads to effects like electromigration, hot carrier degradation, oxide breakedown and electrical over stress.

Hence, it is not prefferred.

(ii) Constant field scaling / Full scaling :-

→ In this case the magnitude of internal electric field in MOSFET remain same while the dimensions are scaled down by a factor 'S'.

→ Hence, the potential also need to be scaled down by 'S'

Quantity before scaling	Quantity after scaling
Gate length, L	$\rightarrow L/S$
Gate width, W	$\rightarrow W/S$
oxide thickness, t_{ox}	$\rightarrow t_{ox}/S$
power supply voltage, V_{DD}	$\rightarrow V_{DD}/S$
Threshold voltage, V_{T_0}	$\rightarrow V_{T_0}/S$
Drain current, I_D	$\rightarrow I_D/S$
power dissipation, P	$\rightarrow P/S^2$
power density, $\frac{P}{A}$	$\rightarrow \frac{P}{A}$

→ We can conclude that, the power density per unit area remain same. Hence, it is preferred over constant voltage scaling.

$$I_D = \frac{\mu_n \epsilon_{ox}}{2 t_{ox}} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D' = \frac{\mu_n \epsilon_{ox}}{2 t_{ox}'} \frac{W'}{L'} (V_{GS} - V_T)^2$$

$$\frac{I_D'}{I_D} = \frac{\frac{\mu_n \epsilon_{ox}}{2 t_{ox}'} \frac{W'}{L'} (V_{GS} - V_T)^2}{\frac{\mu_n \epsilon_{ox}}{2 t_{ox}} \frac{W}{L} (V_{GS} - V_T)^2}$$

$$\Rightarrow I_D' = \frac{1}{S} I_D$$

Short channel effects :- (Small geometry effect)

→ MOSFET will be called as short channel device if it's channel length is same order of magnitude as source and drain depletion region width.

→ It may produce 2 types of effect.

(i) Limitation on electron drift characteristics in the channel

(ii) Modification of threshold voltage due to shortening of channel length

→ The drift velocity in the channel tends to saturate at higher electric field. This phenomenon is called as velocity saturation.

→ In this case, the velocity of carriers doesn't increase with increase in lateral electric field. (Electric field (E_x) across the channel) from source to drain).

(vertical E.F → Gate to substrate) (E_y)

1. velocity saturation
2. mobility degradation
3. channel depletion region charge reduction

Narrow channel effects:-

1. Subthreshold conduction - DIBL, SS
2. Punch through
3. Pin hole - Thinning of t_{ox}
4. Hot electron effect.

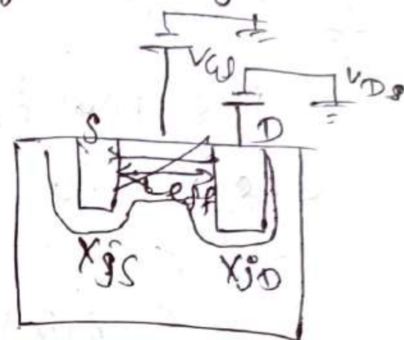
Small geometry effect:-

→ These effects are experienced when MOSFET size is reduced.

→ There are 2 types of small geometry effect.

(i) Short channel effect

(ii) Narrow " "



Short channel effect:-

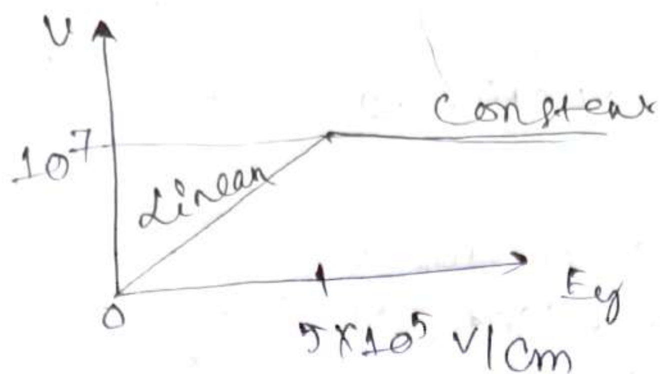
→ When the effective channel length (L_{eff}) is the same order of magnitude as the source and drain junction depth (x_j).

→ There are 3 types of short channel effect.

(i) Velocity saturation:-

Drift velocity v_d for channel $e^{\ominus}$s is proportional to electric field along channel.

$$\uparrow \frac{V_{DS}}{L} = E_y \uparrow = v_d \uparrow \quad (\text{As } v_d = \mu \vec{E_y})$$



→ The velocity get saturated at 10^7 cm/s beyond applied electric field of 5×10^5 V/cm.

(ii) Mobility degradation :-

→ The mobility degrades due to vertical electric field.

$$\mu_{n(eff)} = \frac{\mu_{n0}}{1+\eta (V_{GS}-V_T)}$$

$$V_{GS}-V_T \uparrow \longrightarrow \mu_{n(eff)} \downarrow$$

$$\frac{V_{GS}-V_T}{L} \uparrow \rightarrow \vec{E_x} \uparrow$$

Where, $\eta = \frac{\theta \epsilon_{ox}}{t_{ox} \epsilon_{si}}$

(iii) Channel depletion region charge reduction :

→ The channel length becomes comparable to depletion region charge length.

→ This reduces the effective ~~charge~~ Q_s in channel and threshold voltage is reduced.

Narrow channel effects :-

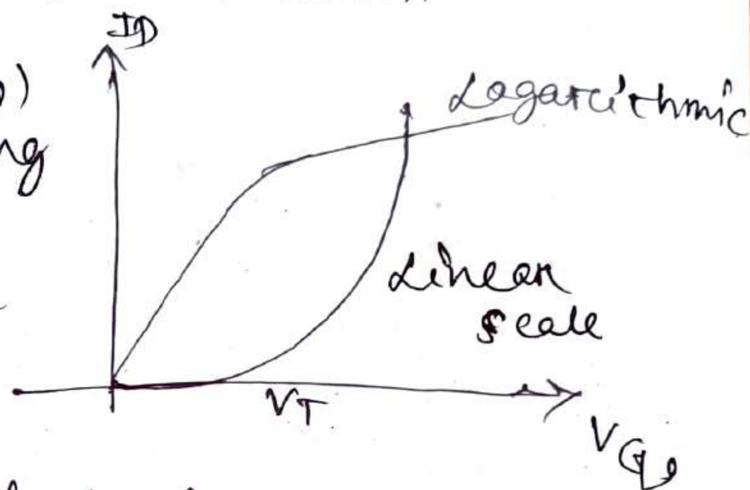
(i) Subthreshold conduction (DIBL, SS) :-

W is on the same order of the maximum depletion region thickness X_{dm}.

Subthreshold → Below threshold voltage

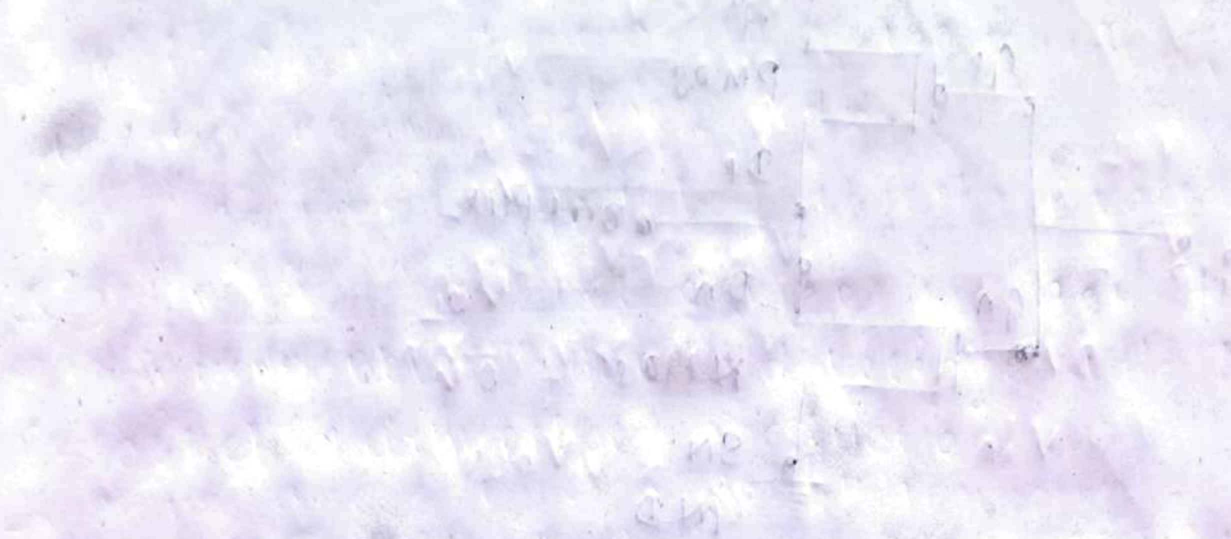
→ In narrow channel devices we get current below threshold voltage, this is called subthreshold conduction.

→ The slope of ($I_D \sim V_{GS}$) characteristics during subthreshold is called subthreshold slope (SS).



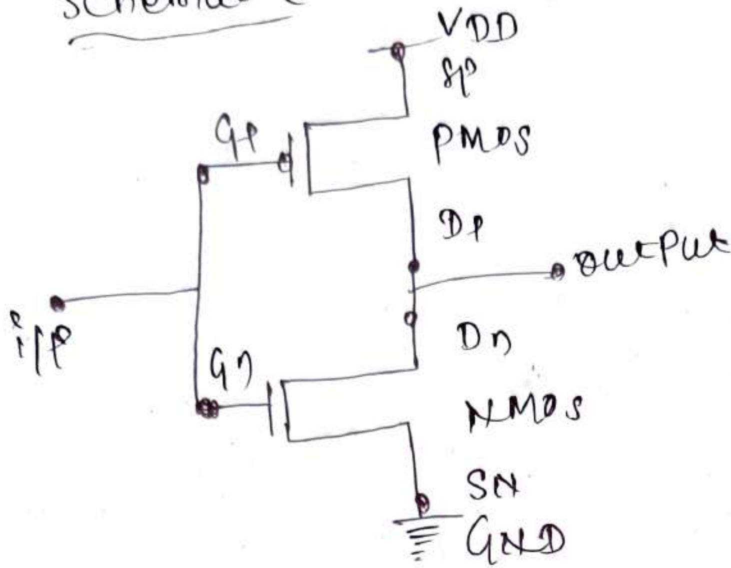
DIBL

In narrow channel devices when drain voltage is increased the drain to source barrier get decreased. So that, e⊖ can easily goes from source to drain even $V_{GS} < V_T$ resulting in drain current. This is called Drain Induced Barrier Lowering.



Layout of CMOS inverter :-

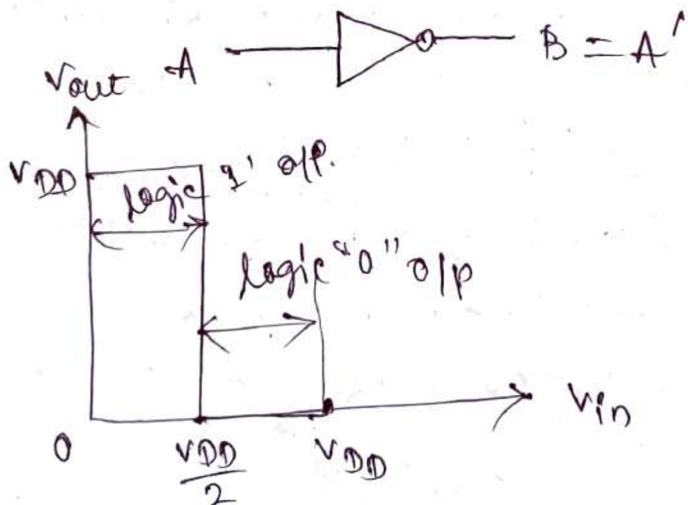
Schematic



Layout :-

→ This a combination of mask ~~representing~~ used during lithography process while fabricating a circuit or device.

inverter :-

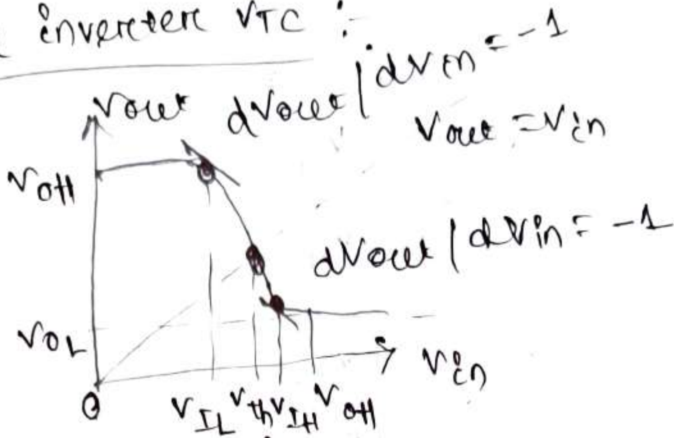


Truth Table

A	B
0	1
1	0

(VTC - voltage transfer characteristics)
ideal inverter VTC

Real inverter VTC :-



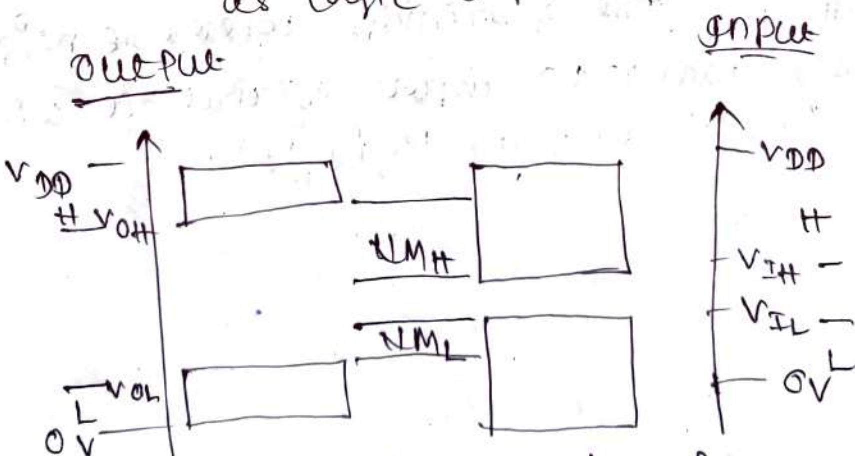
V_{OH} = ~~Maximum~~ Minimum output voltage where input is logic '1'

V_{IL} = Maximum i/p voltage considered as logic '0' corresponding to slope of $V_{TC} = -1$.

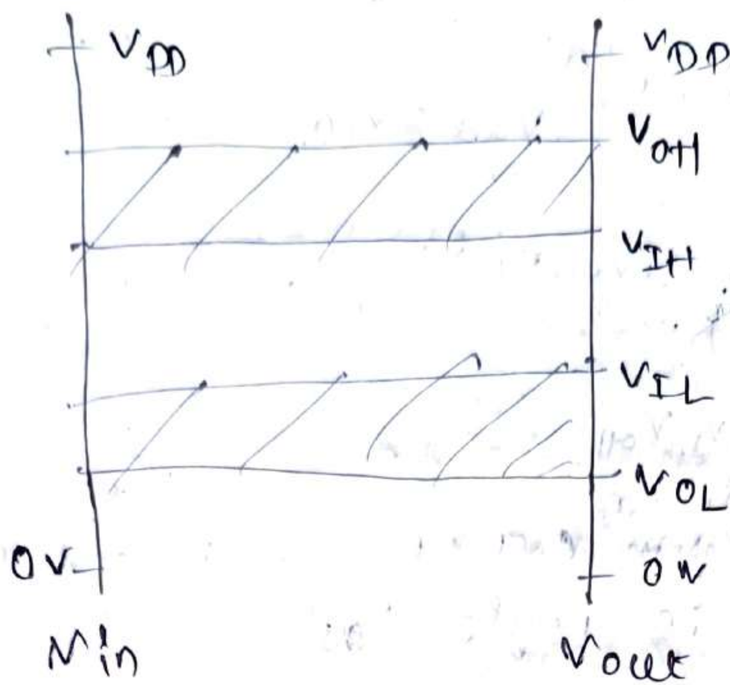
V_{th} = Threshold voltage of inverter representing that i/p voltage equal to output voltage.

V_{IH} = This is the minimum i/p voltage consider as logic '1'.

V_{OL} = Maximum o/p voltage considered as logic '0'.



NM_H = Noise margin High
NM_L = " " Low



$NM_L = V_{IL} - V_{OL}$, $NM_H = V_{OH} - V_{IH}$

→ NM_L is voltage range considered as logic '0'.

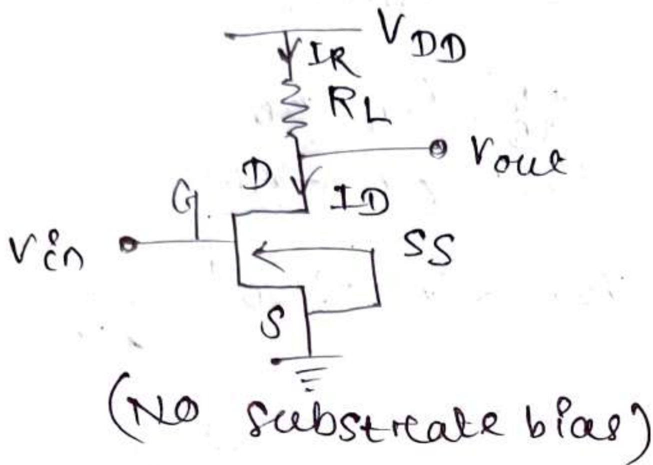
→ NM_H is voltage range considered as logic '1'.

→ NM_L is the maximum tolerable noise voltage added to input so that it will be considered as logic '0'.

→ NM_H is the maximum tolerable noise voltage added to input so that it will be considered as logic '1'.

Inverter with resistive load :-

An NMOS with a resistor connected at the drain as shown in figure can act as an inverter. The resistor act like a load to the transistor.



(NO substrate bias)

$$V_{GS} = V_G - V_S$$
$$= V_{in} - 0$$
$$= V_{in}$$

$$V_{DS} = V_D - V_S$$
$$= V_{out} - 0$$
$$= V_{out}$$

$$V_{out} = V_D = V_{DD} - I_D R_L$$

$$\Rightarrow V_{out} = V_{DD} - I_D R_L$$

$$\Rightarrow I_D R_L = V_{DD} - V_{out}$$

$$\Rightarrow \boxed{I_D = \frac{V_{DD} - V_{out}}{R_L} = I_R}$$

Measuring parameter	condition	NMOS operating mode
V_{OH}	$V_{in} < V_{Tn}$ $I_D = 0$	cut-off
V_{OL}	$V_{out} < V_{in} - V_{Tn}$	linear
V_{IL}	$V_{DD} > V_{IL} - V_{Tn}$ $V_{out} > V_{in} - V_{Tn}$	Saturation
V_{IH}	$V_{out} < V_{in} - V_{Tn}$	linear

V_{OH}

out is high $\cong V_{DD}$

input is low $V_{in} < V_{Tn}$

NMOS is in cut-off mode.

$I_D = 0$

$V_{out} = V_{DD} - I_D R_L$

$\Rightarrow V_{OH} = V_{DD} - 0 \cdot R_L$

$\Rightarrow \boxed{V_{OH} = V_{DD}}$

V_{OL} output is low $\cong 0$

input is high

V_{DS} $\quad V_{GS} - V_{Tn}$

V_{out} $\quad V_{in} - V_{Tn}$

V_{OL} $\quad V_{OH} - V_{Tn}$

$V_{OL} < V_{DD} - V_{Tn}$ (linear)

→ nmos is in linear mode.

$$I_D = \frac{K_n}{2}\left[2(V_{GS}-V_{Tn})V_{DS} - V_{DS}^2\right]$$

$$= \frac{K_n}{2}\left[2(V_{DD}-V_{Tn})V_{OL} - V_{OL}^2\right]$$

$$\Rightarrow \frac{V_{DD}-V_{OL}}{R_L} = \frac{K_n}{2}\left[2(V_{DD}-V_{in})V_{OL} - V_{OL}^2\right]$$

$V_{OL} = V_{DD} + __$ ✗

$= V_{DD} - __$

$$\Rightarrow V_{OL} = V_{DD} - V_{T_0} + \frac{1}{K_n R_L} - \sqrt{\left(V_{DD} - V_{T_0} + \frac{1}{K_n R_L}\right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

V_{IL} $V_{in} = V_{IL}$

$V_{out} \cong V_{OH} \cong V_{DD}$

$V_{DS} > V_{GS} - V_{Tn}$

$V_{DD} > V_{IL} - V_{Tn}$ (saturation)

$$\Rightarrow I_{D(sat)} = \frac{K_n}{2}(V_{GS}-V_{Tn})^2$$

$$\Rightarrow \frac{V_{DD}-V_{out}}{R_L} = \frac{K_n}{2}\left(V_{in}-V_{Tn}\right)^2 \quad \text{--- (1)}$$

Differentiating eqn (1) w.r.t. V_{in}

$$\frac{d\left(\frac{V_{DD}}{R_L} - \frac{V_{out}}{R_L}\right)}{dV_{in}} = \frac{d\left[\frac{K_n}{2}(V_{in}-V_{Tn})^2\right]}{dV_{in}}$$

$$\Rightarrow -\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{K_n}{2}\, 2(V_{in}-V_{Tn})(1-0)$$

$$= K_n(V_{in}-V_{Tn})$$

at $v_{in} = V_{IL}$, $\frac{dV_{out}}{dV_{in}} = -1$

$$\Rightarrow \frac{1}{R_L} = K_n (V_{IL} - V_{Tn})$$

$$\Rightarrow \boxed{V_{IL} = V_{Tn} + \frac{1}{K_n R_L}} \quad (2)$$

putting eq^n (2) in place of v_{in} in eq^n (1)

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2}\left(V_{Tn} + \frac{1}{K_n R_L} - V_{Tn}\right)^2$$

$$= \frac{K_n}{2} \times \frac{1}{K_n^2 R_L^2}$$

$$\Rightarrow V_{DD} - V_{out} = \frac{1}{2 K_n R_L}$$

$$\Rightarrow \boxed{V_{out} = V_{DD} - \frac{1}{2 K_n R_L}}$$

$K_n = \mu_n C_{ox} W/L$

μ_n = mobility of $e^{\ominus}$s in Si

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$. $\frac{\text{Electrical permittivity of oxide}}{\text{thickness oxide}}$

V_{IH}

$v_{in} = V_{IH}$

$\frac{dV_{out}}{dV_{in}} = -1$

$V_{out} \simeq V_{OL}$ $\quad V_{out} > V_{OL}$

V_{DS} $\quad$ $V_{GS} - V_{Tn}$

V_{out} $\quad$ $V_{IH} - V_{Tn}$

$V_{OL} < V_{IH} - V_{Tn}$ (Linear)

$$\Rightarrow I_D = \frac{K_n}{2}\left[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2\right]$$

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2}\left[2(V_{in} - V_{Tn})V_{out} - V_{out}^2\right] \quad \text{--- (1)}$$

diff. eq^n w.r.t. V_{in}

$$\frac{d\left(\frac{V_{DD} - V_{out}}{R_L}\right)}{dV_{in}} = \frac{d\,\frac{K_n}{2}\left[2(V_{in} - V_{Tn})V_{out} - V_{out}^2\right]}{dV_{in}}$$

$$\Rightarrow -\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{K_n}{2}\left[2V_{out} + 2\frac{dV_{out}}{dV_{in}}(V_{in} - V_{Tn}) - 2V_{out}\frac{dV_{out}}{dV_{in}}\right]$$

$$\frac{dV_{out}}{dV_{in}} = -1 \text{ at } V_{in} = V_{IH}$$

$$\Rightarrow \frac{1}{R_L} = K_n\left[V_{out} - (V_{IH} - V_{Tn}) + V_{out}\right]$$

$$\Rightarrow \frac{1}{K_n R_L} = 2V_{out} - V_{IH} + V_{Tn}$$

$$\Rightarrow \boxed{V_{IH} = 2V_{out} + V_{Tn} - \frac{1}{K_n R_L}} \quad \text{--- (2)}$$

Put eqⁿ (3) in eqⁿ (1),

$$\Rightarrow \frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2}\left[2\left(2V_{out} - \frac{1}{K_n R_L}\right) V_{out} - V_{out}^2\right]$$

$$\Rightarrow V_{out} = \sqrt{\frac{2}{3}\frac{V_{DD}}{K_n R_L}}$$

putting value of V_{out} in eqⁿ (2)

$$\Rightarrow V_{IH} = \sqrt{\frac{8}{3}\frac{V_{DD}}{K_n R_L}} + V_{TN} - \frac{1}{K_n R_L}$$

CMOS Inverter :-

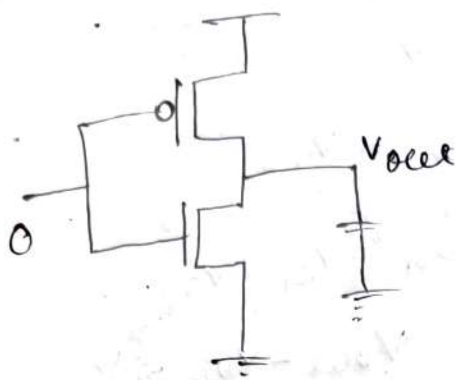
→ In case of inverter with resistive load the output (V_{OH}) is given by,

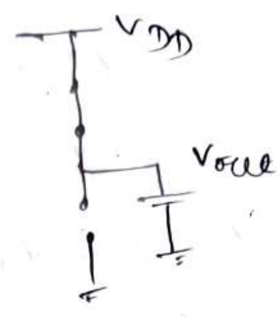
$$V_{OH} = V_{DD} - I_R R_L$$

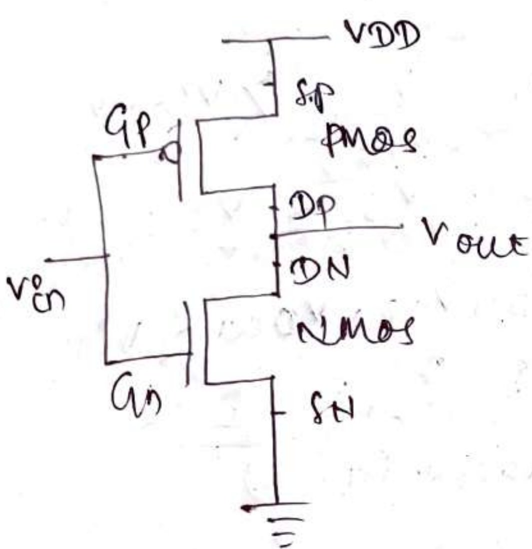
→ In order to get $V_{OH} = V_{DD}$, R_L must be minimum. So, the resistance is replaced by a depletion type MOSFET (Inverter with depletion load)^H.W., OR an NMOS transistor (Inverter with NMOS load)^H.W. OR a PMOS load (CMOS inverter).

Inverter with PMOS load :-

→ In case of CMOS inverter, $V_{OH} = V_{DD}$, $V_{OL} = 0$







$V_{GSP} = V_{GP} - V_{SP}$

$= V_{in} - V_{DD}$

$V_{GSn} = V_{in} - 0 = V_{in}$

$V_{DSP} = V_{DP} - V_{SP}$

$= V_{out} - V_{DD}$

$V_{DSn} = V_{out} - 0 = V_{out}$

NMOS

Cut-off = $V_{GSn} < V_{Tn} \Rightarrow V_{in} < V_{Tn}$

Linear = $V_{GSn} > V_{Tn}$, $V_{DSn} < V_{GSn} - V_{Tn}$

$= V_{in} > V_{Tn}$, $V_{out} < V_{in} - V_{Tn}$

Saturation = $V_{GSn} > V_{Tn}$, $V_{DSn} \geq V_{GSn} - V_{Tn}$

$= V_{in} > V_{Tn}$, $V_{out} \geq V_{in} - V_{Tn}$

PMOS

cut-off $= V_{GSP} > V_{TP}$

$= V_{in} - V_{DD} > V_{TP}$

$= V_{in} > V_{DD} + V_{TP}$

linear $= V_{GSP} < V_{TP}$, $V_{DSP} > V_{GSP} - V_{TP}$

$= V_{in} - V_{DD} < V_{TP}$, $V_{out} - V_{DD} > V_{in} - V_{DD} - V_{TP}$

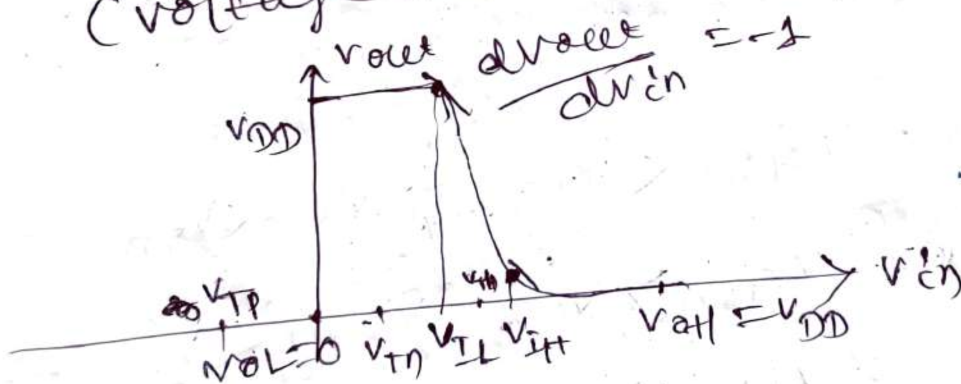
$= V_{in} < V_{DD} + V_{TP}$, $V_{out} > V_{in} - V_{TP}$

saturation $= V_{GS} \leq V_{TP}$, $V_{DS} \leq V_{GSP} - V_{TP}$

$= V_{in} \leq V_{DD} + V_{TP}$, $V_{out} \leq V_{in} - V_{TP}$

VTC of CMOS inverter :-

(voltage transfer characteristics)



(A) $V_{in} < V_{Tn}$

NMOS : cut-off

PMOS linear

$V_{in} = 0.5$ V (let)

$V_{DD} + V_{TP} = 5 - 1 = 4$ V

$V_{in} - V_{TP} = 0.5 + 1 = 1.5$

$V_{out} = V_{DD} = 5$

(B) $V_{in} = V_{IL} = 2$ (Let)

NMOS (Saturation) $V_{in} > V_{Tn}$

$V_{out} \quad V_{in} - V_{Tn}$

$4.5 > 1$

PMOS (linear)

$V_{in} < V_{Tp} + V_{DD}$

$2 < -1 + 5$

$2 < 4$

$V_{out} > V_{in} - V_{Tp}$

$4.5 \quad 2 + 1$

$4.5 > 3$

$V_{DD} -$
V_{Tp}
P
V_{Tp}
$-V_{Tp}$

Calculation of V_{IL} and V_{IH} :- (B)

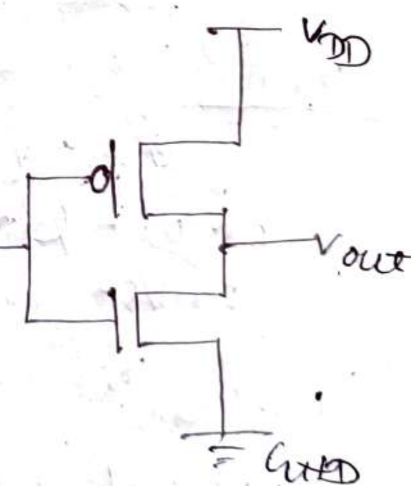
(D)

V_{IL} PMOS - linear

NMOS - saturation

$V_{in} = V_{IL}$, $\frac{dV_{out}}{dV_{in}} = -1$

I_{Dp} (linear) = I_{Dn} (saturation)



$\Rightarrow \frac{K_P}{2}\left[2(V_{GSp} - V_{Tp})V_{DSp} - V_{DSp}^2\right]$

$= \frac{K_n}{2}\left[(V_{GSn} - V_{Tn})^2\right]$

$\Rightarrow K_P\left(2(V_{in} - V_{DD} - V_{Tp})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right)$

$= K_n (V_{in} - V_{Tn})^2$ ———— (1)

Differentiate eqn (1) w.r.t V_{in},

$$\Rightarrow K_p \left(2\left[(1)(V_{out} - V_{DD}) + \left(\frac{dV_{out}}{dV_{in}} - 0\right)(V_{in} - V_{DD} - V_{Tp}) \right] \right.$$

$$2(V_{out} - V_{DD})\left(\frac{dV_{out}}{dV_{in}}\right) = K_n \, 2(V_{in} - V_{Tn})(1)$$

$$\Rightarrow K_p \left[2(V_{out} - V_{DD} - V_{in} + V_{DD} + V_{Tp}) + 2(V_{out} - V_{DD}) \right] = K_n \, 2(V_{in} - V_{Tn})$$

$$\Rightarrow K_p (2V_{out} - 2V_{in} + 2V_{Tp} + 2V_{out} - 2V_{DD}) = K_n(2V_{in} - 2V_{Tn})$$

$$K_R = \frac{K_n}{K_p}$$

$$\Rightarrow \frac{K_n}{K_p}(V_{IL} - V_{Tn}) = 2V_{out} - V_{IL} + V_{Tp} - V_{DD}$$

$$\Rightarrow \boxed{V_{IL} = \frac{2V_{out} + V_{Tp} - V_{DD} + K_R V_{Tn}}{(1 + K_R)}} \quad \text{--- (2)}$$

put eq^n (2) in place of V_{in} in eq^n (1),

$\underline{V_{IH}}$ $\boxed{\quad}$ --- (3)

$V_{in} = V_{IH}$

nmos - linear

pmos - saturation.

$$I_{Dn}(lin) = I_{Dp}(sat)$$

$$\Rightarrow \frac{K_n}{2}\left[2(V_{GSn} - V_{Tn})V_{DSn} - V_{DSn}^2 \right] = \frac{K_p}{2}\left[(V_{GSp} - V_{Tp})^2 \right]$$

$$\Rightarrow K_R \left[2 (V_{in} - V_{TN}) V_{out} - V_{out}^2 \right] = (V_{in} - V_{DD} - V_{TP})^2 \quad \text{--- (4)}$$

Differentiating eq^n (4) w.r.t V_{in}

$$\Rightarrow K_R \left(2 \left[1 \cdot V_{out} + \frac{dV_{out}}{dV_{in}} (V_{in} - V_{TN}) \right] - 2 V_{out} \frac{dV_{out}}{dV_{in}} \right) = 2 (V_{in} - V_{DD} - V_{TP}) (1)$$

$$\Rightarrow K_R \left[V_{out} - V_{in} + V_{TN} + V_{out} \right] = V_{in} - V_{DD} - V_{TP}$$

$$\Rightarrow K_R (2V_{out} - V_{IH} + V_{TN}) = V_{IH} - V_{DD} - V_{TP}$$

$$\Rightarrow 2K_R V_{out} - K_R V_{IH} + K_R V_{TN} - V_{IH} + V_{DD} + V_{TP} = 0$$

$$\Rightarrow V_{IH} = \frac{2K_R V_{out} + K_R V_{TN} + V_{DD} + V_{TP}}{1 + K_R}$$

$$\Rightarrow \boxed{V_{IH} = \frac{V_{DD} + V_{TP} + K_R (2V_{out} + V_{TN})}{1 + K_R}} \quad \text{--- (5)}$$

putting eq^n (5) in place of V_{in} eq^n (4)

$$V_{out} = \quad \text{--- (6)}$$

Calculation of V_{th} :-

V_{th} = Threshold voltage of inverter

at $V_{in} = V_{th} = V_{out}$

at region ©

both pmos and nmos are in saturation mode, $V_{in} = V_{th}$.

$I_{Dn}(sat) = I_{Dp}(sat)$

$$\Rightarrow \frac{K_n}{2}(V_{GSn} - V_{Tn})^2 = \frac{K_p}{2}(V_{GSp} - V_{Tp})^2$$

$$\Rightarrow K_R(V_{in} - V_{Tn})^2 = (V_{in} - V_{DD} - V_{Tp})^2$$

$$\Rightarrow K_R(V_{th} - V_{Tn})^2 = (V_{th} - V_{DD} - V_{Tp})^2 \quad (V_{Tn} - V_{th})$$

$$\Rightarrow \sqrt{K_R}(V_{th} - V_{Tn}) = V_{th} - V_{DD} - V_{Tp}$$

$$\Rightarrow V_{th} - \sqrt{K_R}V_{th} = V_{DD} + V_{Tp} - \sqrt{K_R}V_{Tn}$$

$$\Rightarrow \boxed{V_{th} = \frac{V_{DD} + V_{Tp} - \sqrt{K_R}V_{Tn}}{1 - \sqrt{K_R}}} \quad \text{or}$$

$$\Rightarrow \boxed{V_{th} = \frac{V_{Tn} + \frac{1}{\sqrt{K_R}}(V_{DD} + V_{Tp})}{1 + \frac{1}{\sqrt{K_R}}}} \quad -(1)$$

$$\boxed{V_{th} = \frac{V_{DD} + V_{Tp} + \sqrt{K_R}V_{Tn}}{1 + \sqrt{K_R}}} \quad -(2)$$

for special case, $\boxed{V_{th} = \frac{V_{DD}}{2}}$

$$\Rightarrow \frac{V_{DD}}{2} = \frac{\sqrt{K_R}\, V_{Tn} + V_{DD} + V_{Tp}}{\sqrt{K_R} + 1}$$

$$\Rightarrow 2\sqrt{K_R}\, V_{Tn} + 2V_{DD} + 2V_{Tp} = \sqrt{K_R}\, V_{DD} + V_{DD}$$

$$\Rightarrow \sqrt{K_R}\,(V_{DD} - 2V_{Tn}) = V_{DD} + 2V_{Tp}$$

$$\Rightarrow \sqrt{K_R} = \frac{V_{DD} + 2V_{Tp}}{V_{DD} - 2V_{Tn}}$$

$$\Rightarrow \boxed{\sqrt{K_R} = 2\left(\frac{\frac{V_{DD}}{2} + V_{Tp}}{\frac{V_{DD}}{2} - V_{Tn}}\right)}$$

$\Rightarrow$ If, $|V_{Tp}| = |V_{Tn}|$

$\boxed{K_R = 1}$

Put $K_R = 1$

$$\Rightarrow V_{out} = \frac{V_{DD}}{2}$$

Put $K_R = 1$ and $V_{out} = \frac{V_{DD}}{2}$ in eq^n (3) & (4),

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{Tn})$$

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_{Tn})$$

This cond^n is satisfied only in case of of inverter. $\boxed{V_{DD} = V_{IL} + V_{IH}}$

$NM_L = V_{IL}$

$NM_H = V_{DD} - V_{IH} = V_{IL}$

$K_R = 1$ when $V_{th} = \frac{V_{DD}}{2}$ → symmetric inverter

$\Rightarrow \frac{K_n}{K_p} = 1$

$\Rightarrow \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = 1$

$\Rightarrow \frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n}$

for a particular technology, $L_n = L_p$

L_n = gate length of NMOS

L_p = gate length of PMOS

W_n = gate width of NMOS

W_p = gate width of PMOS

$\Rightarrow \frac{W_n}{W_p} = \frac{\mu_p}{\mu_n}$ $\because \mu_n \cong 2.5 \mu_p$

$\Rightarrow \frac{W_n}{W_p} = \frac{1}{2.5}$

$\Rightarrow \boxed{W_p = 2.5 W_n}$

∴ PMOS is bigger in size.

Q. Consider a CMOS inverter circuit with the following parameters.

$V_{DD} = 3.3V$ $K_n = 200 \mu A/V^2$

$V_{TO,n} = 0.6V$ $K_p = 80 \mu A/V^2$

$V_{TO,p} = -0.7V$

Calculate the noise margin.

Sol^n $V_{OL} = 0\ V$

$V_{OH} = V_{DD} = 3.3V$ $K_R = \frac{K_n}{K_p} = 2.5$

$V_{IL} = ?$, $V_{IH} = ?$

$$V_{IL} = \frac{2V_{out} + V_{Tp} - V_{DD} + K_R V_{Tn}}{1 + K_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + 2.5 \times 0.6}{1 + 2.5}$$

$$V_{IL} = \frac{2V_{out} - 2.5}{3.5}$$

from eq^n (1).

$$K_p\left[2(V_{IL} - V_{DD} - V_{Tp})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right] = K_n (V_{IL} - V_{Tn})^2$$

$$\Rightarrow 2(V_{IL} - 3.3 + 0.7)(V_{out} - 3.3) - (V_{out} - 3.3)^2 = 2.5(V_{IL} - 0.6)^2$$

$$\Rightarrow 2\left(\frac{2V_{out} - 2.5}{3.5} - 2.6\right)(V_{out} - 3.3) - (V_{out} - 3.3)^2 = 2.5\left(\frac{2V_{out} - 2.5}{3.5} - 0.6\right)^2$$

$$\Rightarrow 2\left(\frac{2V_{out}-2.5-9.1}{3.5}\right)(V_{out}-3.3)-(V_{out}-3.3)^2$$

$$= 2.5\left(\frac{2V_{out}-2.5-2.1}{3.5}\right)^2$$

$$\Rightarrow \frac{2}{3.5}(2V_{out}-11.6)(V_{out}-3.3)-$$

$$(V_{out}-3.3)^2 = \frac{2.5}{(3.5)^2}(2V_{out}-4.6)^2$$

$$\Rightarrow 0.571\,(2V_{out}^2-6.6V_{out}-11.6V_{out}+38.28)-(V_{out}^2+10.89-6.6V_{out})$$

$$= 0.204\,(4V_{out}^2+21.16-18.4V_{out})$$

$$\Rightarrow 1.142V_{out}^2 - 10.3922V_{out} + 21.857 - V_{out}^2 - 10.89 + 6.6V_{out}$$

$$- 0.816V_{out}^2 - 4.316 + 3.75V_{out} = 0$$

$$\Rightarrow -0.674V_{out}^2 - 0.05V_{out} + 6.65 = 0$$

$$\Rightarrow 0.674V_{out}^2 + 0.05V_{out} - 6.65 = 0$$

$V_{out} = 3.104$ V

-3.178 V

$$\Rightarrow \boxed{V_{IL} = 1.06\text{ V}}$$

VII Va
1.08
03.11

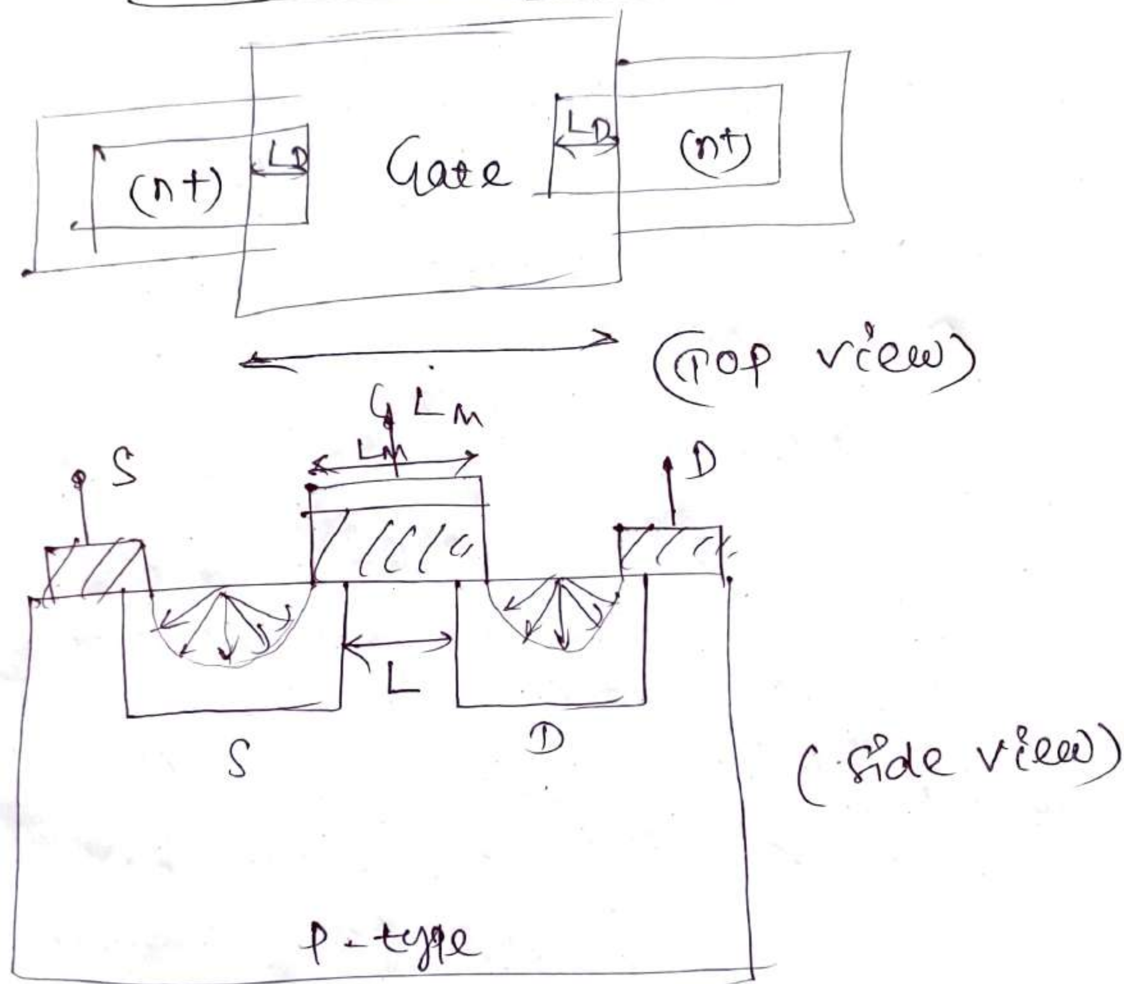
MOSFET capacitance :-

→ There are 3 types of capacitance found in MOSFET ~~mainly~~.

① overlap capacitance ③ Junction capacitance

② capacitance due to channel charge

Overlap capacitance :-



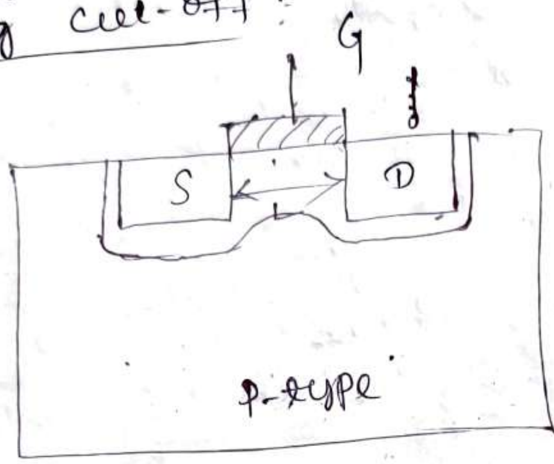
→ The capacitance formed due to overlapping of gate on source and drain region ~~due to~~ during doping is called overlapping capacitance.

→ It is given by $C_{GS} = C_{GD} = C_{ox} W . L_D$

Capacitance due to channel charge :

→ This capacitance is formed due to overlapping of gate on substrate or body through oxide.

During cut-off :

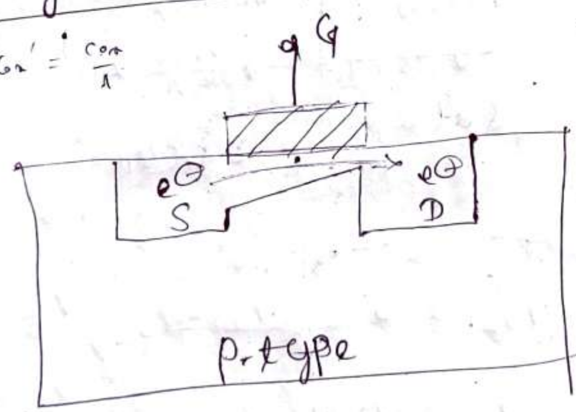


$C_{gs} = C_{gd} = 0$

$C_{gb} = C_{ox} \cdot \omega \cdot L$

During linear :

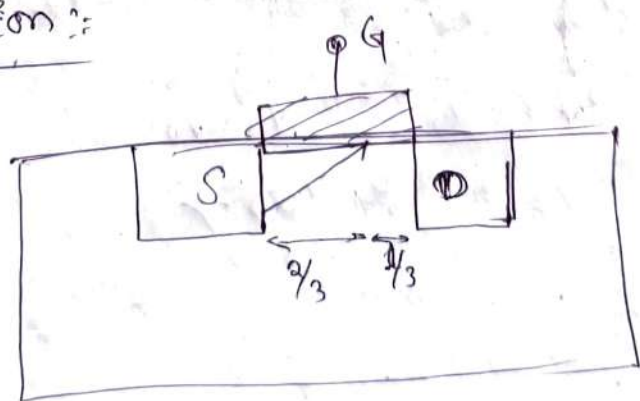
$C_{ox}' = \frac{C_{ox}}{A}$



$C_{gd} = C_{gs} = C_{ox} \cdot \omega \cdot \frac{L}{2}$

$C_{gb} = 0$

During Saturation :

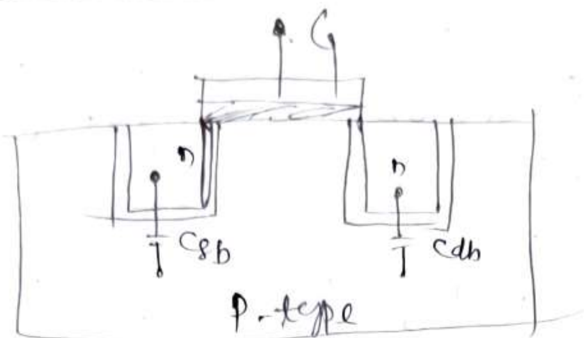


$C_{gs} = C_{ox} \cdot \omega \cdot \frac{2L}{3}$

$C_{gd} = 0$

$C_{gb} = 0$

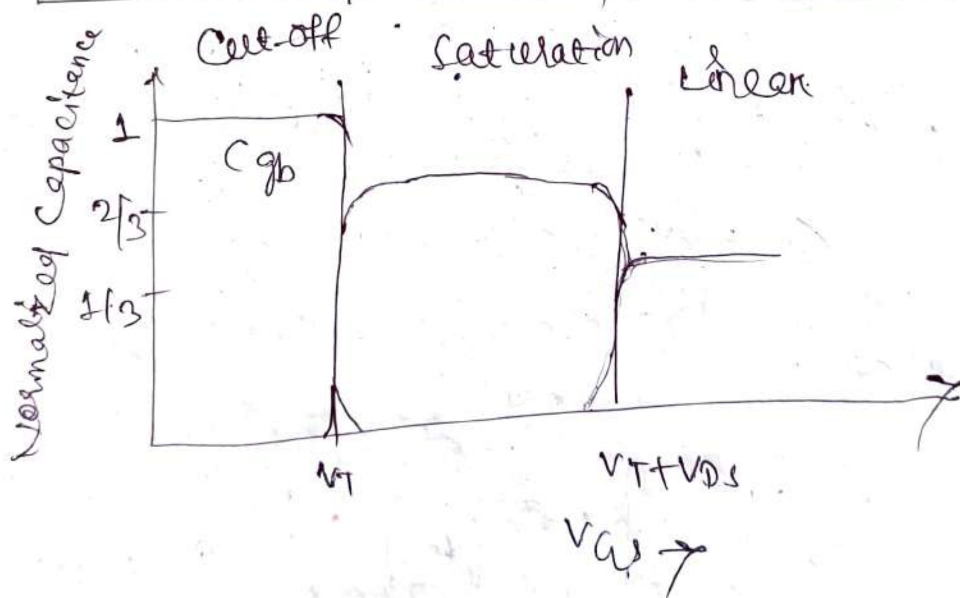
Junction capacitance:



$C_{gd} = L_D, L_D/2$

$C_{gs} = L_D, L/2$

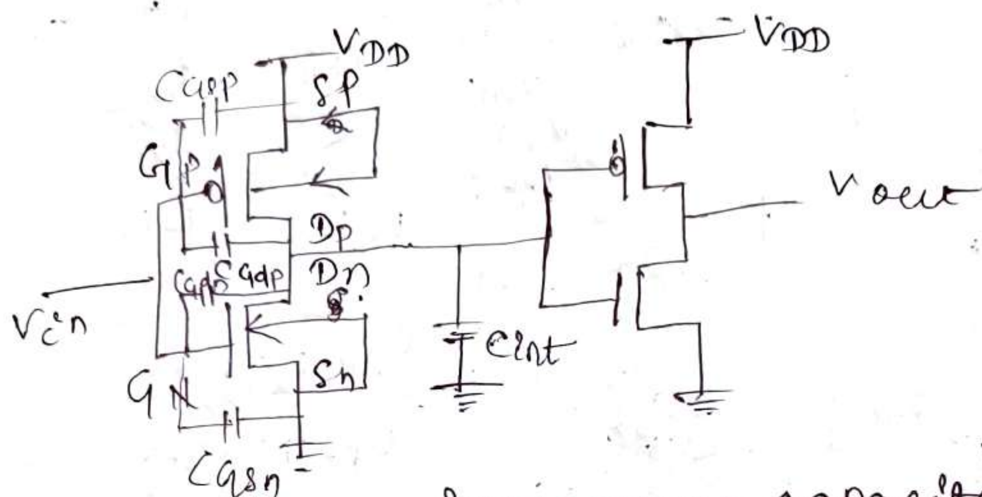
Capacitance	Cut-off	Linear	Saturation
Cgb (total)	$C_{ox}WL$	0	0
Cgd (total)	$C_{ox}WL_D$	$C_{ox}WL/2 + C_{ox}WL_D$	$C_{ox}WL_D$
Cgs (total)	$C_{ox}WL_D$	$C_{ox}WL/2 + C_{ox}WL_D$	$2C_{ox}WL/3 + C_{ox}WL_D$



Delay time analysis of inverter:

→ When inverters are connected back to back in VLSI circuits, the signal propagation faces delay due to capacitances involved along with inverter.

→ The different capacitances involved along with inverter can be shown as figure.

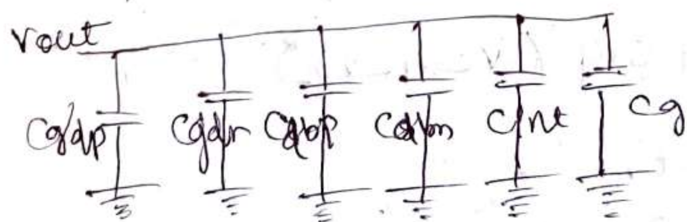


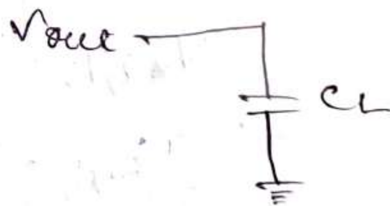
C_{int} – interconnect capacitance

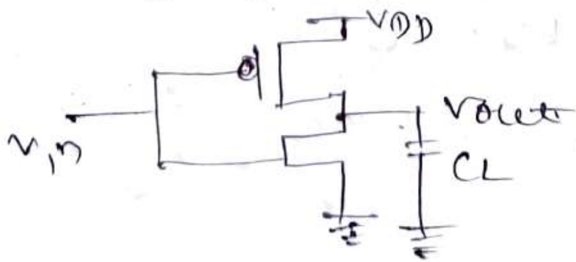
Intrinsic capacitance = $C_{gd,p} + C_{gd,n} + C_{db,p} + C_{db,n}$

Extrinsic " = $C_{int} + C_g$

$$C_{load} = C_{gd,p} + C_{gd,n} + C_{db,p} + C_{db,n} + C_{int} + C_g$$



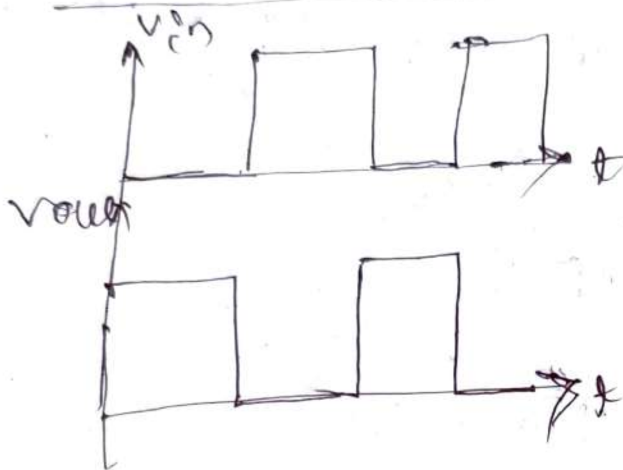


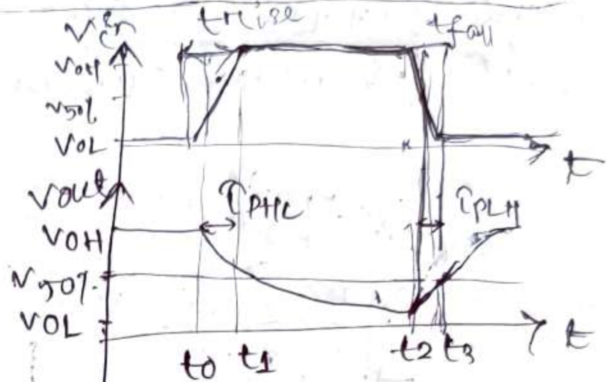


→ This load capacitance provides intermediate delay between two inverter circuit.

→ ~~Due to~~ Also it provides propagation delay from i/p of inverter to o/p of inverter.

Ideal inverter i/p and o/p characteristics:

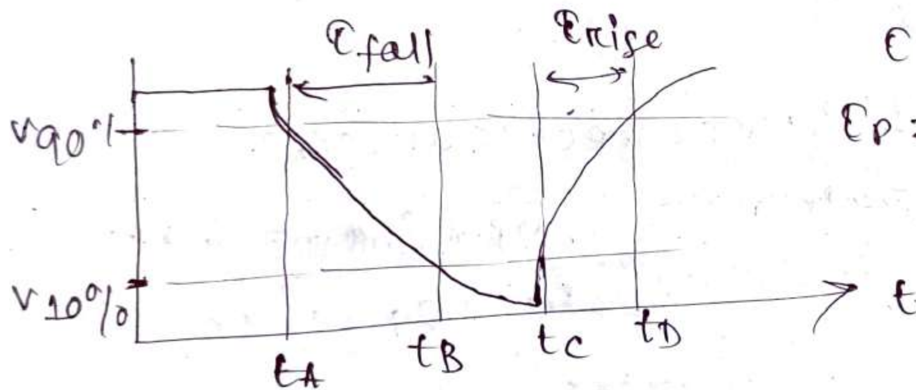




$\tau_{PHL} = t_1 - t_0$

$\tau_{PLH} = t_3 - t_2$

$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$



$V_{10\%} = V_{OL} + 0.1\,(V_{OH} - V_{OL})$

$V_{90\%} = V_{OL} + 0.9\,(V_{OH} - V_{OL})$

$\tau_{fall} = t_B - t_A$

$\tau_{rise} = t_D - t_C$

$$\tau_{PHL} = \frac{C_{load}(V_{OH} - V_{50\%})}{I_{avg.HL}}$$

$$\tau_{PLH} = \frac{C_{load}(V_{50\%} - V_{OL})}{I_{avg.LH}}$$

Where,

$$I_{avg.HL} = \frac{1}{2}\left[i_c(V_{in}=V_{OH}, V_{out}=V_{OH}) + i_c(V_{in}=V_{OH}, V_{out}=V_{50\%})\right]$$

$$I_{avg.LH} = \frac{1}{2}\left[i_c(V_{in}=V_{OL}, V_{out}=V_{50\%}) + i_c(V_{in}=V_{OL}, V_{out}=V_{OL})\right].$$

$$dq = i\,dt = c\,dv$$

$$\Rightarrow \int dt = \frac{c}{i}\int dv$$

$$\Rightarrow \tau_{PHL} = \frac{C_L(V_{OH} - V_{50\%})}{i_{avg.HL}}$$

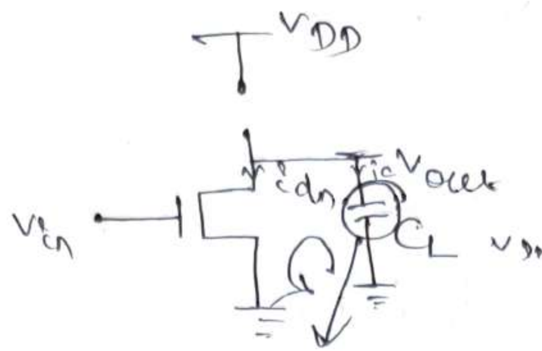
$$i_{avg,HL} = \frac{i(V_{OH}) + i(V_{50\%})}{2}$$

Calculation of τ_{PHL} :-

at τ_{PHL}, V_{out} changes from V_{OH} to V_{OL}

V_{in} changes from V_{OL} to V_{OH}

If $V_{in} = V_{OH}$, PMOS = Off (cut-off), NMOS = ON (Lin/sat)



$i_c = -i_{d,n}$

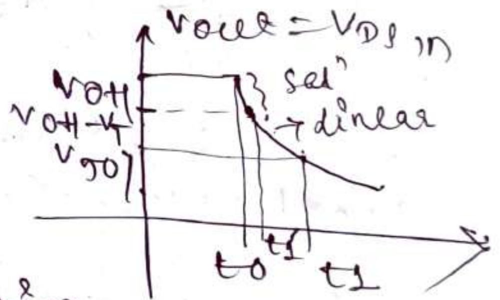
(Capacitor acts as a voltage source)

$C_{out}\, dV_{out} = i_c\, dt$

$\Rightarrow i_c = C_{out} \frac{dV_{out}}{dt}$

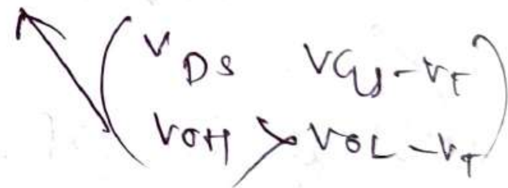
$\Rightarrow -i_{d,n} = C_{out}\left(\frac{dV_{out}}{dt}\right)$

$i_{d,n} = i_{d,lin} / i_{d,sat^n}$.



$t_{PHL} = t_1 - t_0$

at $t = t_0$, NMOS is in saturation



$$\begin{pmatrix} V_{DS} & V_{GS} - V_T \\ V_{OH} - V_T = & V_{OH} - V_T \\ & < \end{pmatrix}$$

t_0 to t_1' = NMOS is in saturation

t_1' to t_1 = NMOS is in linear.

$$C\frac{dv}{dt} = -i_{d,n}$$

$$\Rightarrow \int C\,dv = -\int i_{d,n}\,dt$$

Time interval

for t_0 to t_1'

$$\int_{V_{OH}}^{V_{OH}-V_T} C\,dv = -\int_{t_0}^{t_1'} i_{d,n}\,dt$$

$$\Rightarrow C\,(V_{OH} - V_T - V_{OH}) = -\frac{k_n}{2}(V_{OH}-V_T)^2\,(t_1' - t_0)$$

$$i_{d,sat} = \frac{k_n}{2}(V_{GS}-V_T)^2 = \frac{k_n}{2}(V_{OH}-V_T)^2$$

$$\Rightarrow \boxed{t_1' - t_0 = \frac{2\,C_{Load}\,V_T}{k_n\,(V_{OH}-V_T)^2}}$$

for t_1' to t_1

$$\int_{V_{OH}-V_T}^{V_{50\%}} C\,dv = -\int_{t_1'}^{t_1} i_{d,n}\,dt$$

$$i_{d,lin} = \frac{k_n}{2}\left[2(V_{GS}-V_T)^2 V_{out} - V_{out}^2\right]$$

$$\Rightarrow \int_{V_{OH}-V_T}^{V_{50\%}} C\,\frac{dV_{out}}{i_{d,n}} = -\int_{t_1'}^{t_1} dt$$

$$\Rightarrow C\int_{V_{OH}-V_T}^{V_{50\%}} \frac{2\,dV_{out}}{k_n\left[2(V_{OH}-V_T)V_{out}-V_{out}^2\right]} = -(t_1-t_1')$$

$$\Rightarrow \frac{2C}{k_n}\int_{V_{OH}-V_T}^{V_{50\%}} \frac{dV_{out}}{2(V_{OH}-V_T)V_{out}-V_{out}^2} = -(t_1-t_1')$$

~~$\Rightarrow \frac{2C}{k_n}\left(\int \frac{dV_{out}}{2(V_{OH}-V_T)V_{out}} - \int \frac{dV_{out}}{V_{out}^2}\right) = -(t_1-t_1')$~~

~~$\Rightarrow \frac{2C}{k_n}\,\frac{1}{2(V_{OH}-V_T)}$~~

$$\Rightarrow \frac{2C}{k_n}\left(2(V_{OH}-V_T)-2V_{out}\right)dV_{out}$$

⋮

$$\Rightarrow t_1-t_1' = -\frac{2C_{load}}{k_n}\,\frac{1}{2(V_{OH}-V_{T,n})}\ln\left(\frac{V_{out}}{2(V_{OH}-V_T)-V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_T}^{V_{out}=V_{50\%}}$$

$$\boxed{\Rightarrow t_1-t_1' = \frac{C_{load}}{k_n(V_{DD}-V_T)}\ln\left(\frac{4(V_{OH}-V_T)}{V_{50\%}}\right)}$$

$\therefore \tau_{PHL} = (t_1' - t_0) + (t_1 - t_1')$

$$= \frac{C_{Load}}{K_n (V_{OH} - V_T)} \left[\frac{2V_T}{V_{OH} - V_T} + \ln\left(\frac{4(V_{OH} - V_T)}{V_{OH} + V_{OL}} - 1 \right) \right]$$

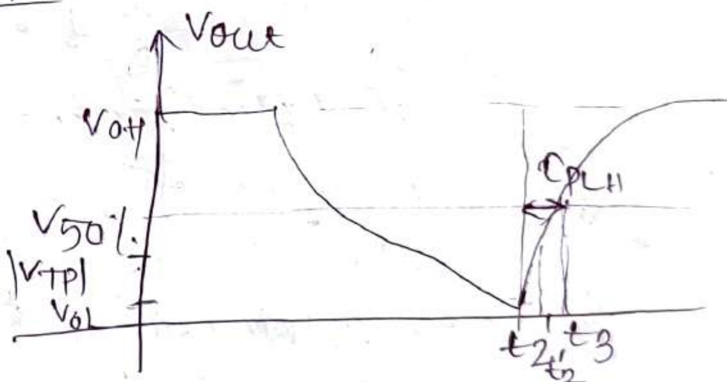
$V_{OH} = V_{DD}$

$V_{OL} = 0$

$V_{50\%} = \frac{V_{OH} + V_{OL}}{2}$

$$\Rightarrow \tau_{PHL} = \frac{C_{load}}{K_n (V_{DD} - V_T)} \left[\frac{2V_T}{V_{DD} - V_T} + \ln\left(\frac{4(V_{DD} - V_T)}{V_{DD}} - 1 \right) \right]$$

Calculation of τ_{PLH} :-



$V_{out} \rightarrow$ low to High

$V_{in} \rightarrow$ High to low

1 to 0

PMOS = ON

NMOS = OFF

$i_{d,p} = i_c$

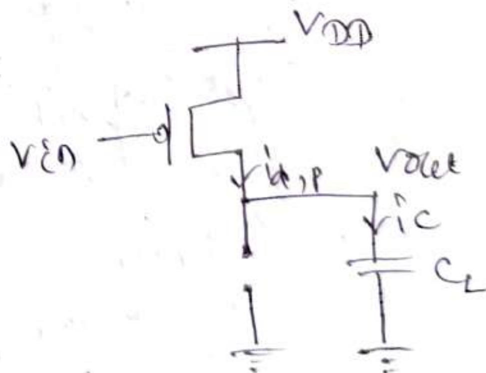
PMOS = Linear / saturation

t_2 to t_2'

$0 - |V_{TP}|$

V_{DS} $V_{GS} - V_{TP}$

V_{out} $\geq$ $V_{in} - V_{TP}$



(linear)

$0 > -1 \Leftarrow V_{OL}\ (0) > V_{DD} - V_{TP}\ (0-1)$

t_2' to t_3

$V_{DS} < V_{GS} - V_{Tp}$ (saturation)

For t_2 to t_2' (PMOS is in Linear)

$$C\,dV = i\,dt$$

$$\Rightarrow \frac{C\,dV}{i_{dp}} = dt$$

$$\Rightarrow \int_0^{|V_{Tp}|} \frac{C}{i_{dp}}\,dV = \int_{t_2}^{t_2'} dt$$

$$i_{dp_{lin}} = \frac{K_p}{2}\left[2\left(V_{OL} - V_{Tp}\right)V_{out} - V_{out}^2\right]$$

$$\Rightarrow t_2' - t_2 = \int_0^{|V_{Tp}|} \frac{C\,dV_{out}}{\frac{K_p}{2}\left(2\left(V_{OL} - V_{Tp}\right)V_{out} - V_{out}^2\right)}$$

For t_2' to t_3 (PMOS is in saturation)

$$\int C\frac{dV}{i_{dp}} = \int dt$$

$$\Rightarrow \int_{|V_{Tp}|}^{V_{50\%}} C\frac{dV}{i_{dp}} = \int_{t_2'}^{t_3} dt$$

$$i_{dp_{sat}} = \frac{K_p}{2}\left(V_{GS} - V_{Tp}\right)^2$$

$$= \frac{K_p}{2}\left(V_{OL} - V_{Tp}\right)^2$$

$\Rightarrow t_3 - t_2' = \frac{c\,dV}{}$

$\therefore \tau_{PLH} = (t_2' - t_2) + (t_3 - t_2')$

$$\boxed{\tau_{PLH} = \frac{C_{load}}{K_p(V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]}$$

Design aspects for lower propagation delay:

$$\tau_p = \frac{C \Delta V}{I_d}$$

τ_p to be small.

C should decrease.

i_d can increase. ($\omega \uparrow$)

- ✓ → increase transistor size.
- ✓ → keep capacitance small.
- → increase V_{DD} ($\uparrow P_{static} = I_D V_{DD} \uparrow$) ✗

Dynamic power dissipation :-

→ It can be defined as the product of average drain current and VDD.

$$P_{dyn,avg} = V_{DD} I_{D,avg}$$

$$I_D = C_{load} \frac{dV_{out}}{dt}$$

$$\Rightarrow \int_0^T I_D\,dt = \int_0^{V_{DD}} C_{load}\,dV_{out}$$

$$\Rightarrow I_{D,avg} T = C_{load} V_{DD}$$

$$\Rightarrow I_{D,avg} = \frac{C_L V_{DD}}{T}$$

$$\Rightarrow I_{D,avg} = C_L V_{DD} f$$

$$\therefore P_{dynamic} = I_{D,avg} \cdot V_{DD}$$

$$\Rightarrow P_{dyn} = C_L V_{DD} f V_{DD}$$

$$\Rightarrow \boxed{P_{dynamic} = C_L V_{DD}^2 f}$$

$$\boxed{P_{static} = I_D V_{DD}}$$

Interconnect analysis :-

→ While fabricating an IC using CMOS technology many metal layers are used.

→ When these layers overlap through some dielectric they produce some unintensional capacitance.

→ Metal layers produce some resistance due to inherant resistivity.

→ Hence, unintensionally we get RC network and this provides delay in the circuit.
→ These ~~RC combination~~ delay can be model by many models but particularly the model will read here is Elmore model.

Interconnect resistance :-

$$R = \frac{\rho l}{A}$$

l = length of metal layer

A = Area of cross-section of metal layer.

$= t \cdot w$

t = thickness of metal layer

= constant for a fabrication process

$$R = \frac{\rho}{t} \cdot \frac{l}{w} \qquad R_\square = \text{sheet resistance}$$

$$\Rightarrow \boxed{R = R_\square \frac{l}{w}}$$

Q. The resistance of a particular metal is given by 1 kΩ, if the metal layer is fabricated for a length of 500 nm and width of 180 nm. What is the resistance offered by the metal layer? If the resistivity of the metal layer is ~~...~~ 10^{-6} Ωm, determine the thickness of metal layer to be deposited.

Sol^n $R_\square = 1$ kΩ, $l = 500$ nm, $w = 180$ nm

$$R = R_\square \frac{l}{w} = 2.77 \text{ k}\Omega$$

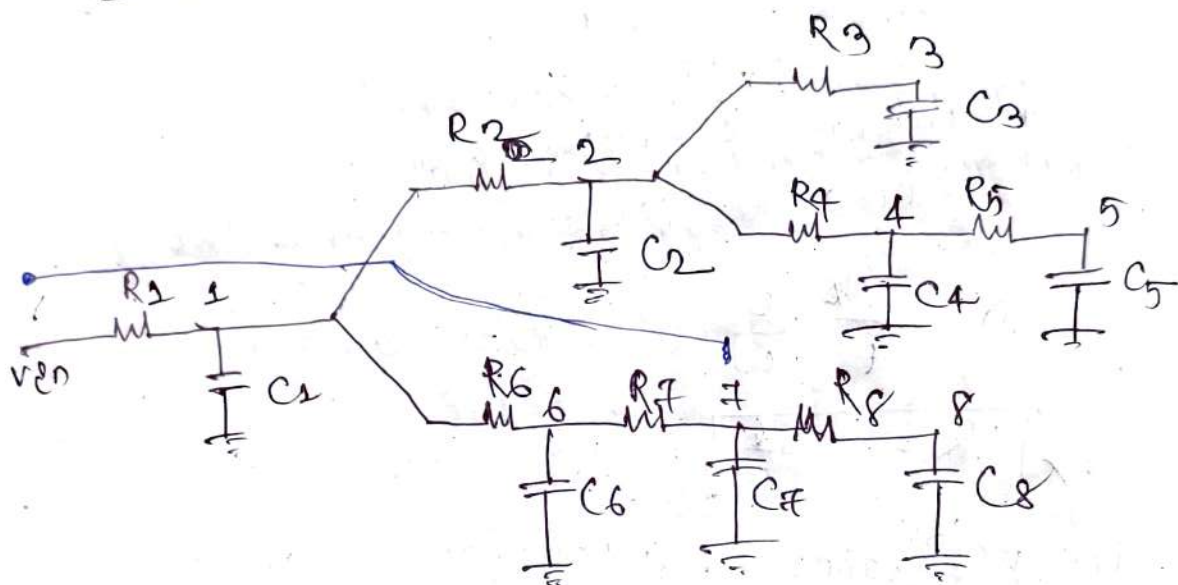
$$\rho = 10^{-6}\ \Omega m \Rightarrow R = \frac{\rho}{t}\frac{l}{w}$$

$$\Rightarrow t = \frac{\rho}{R}\frac{l}{w} = 1 \text{ nm}$$

Computation of Elmore delay :-

→ This model is used to calculate the delay between initial node and any other node of a network consisting of series combination of R & C elements as shown in figure.

Step-1 Find the shortest path between initial load and node at which delay is to be calculated from the initial load.



Step-2

For the nodes not coming on the shortest path, the delay is given by product of addition of all resistances present in the shortest path and capacitance at that particular node.

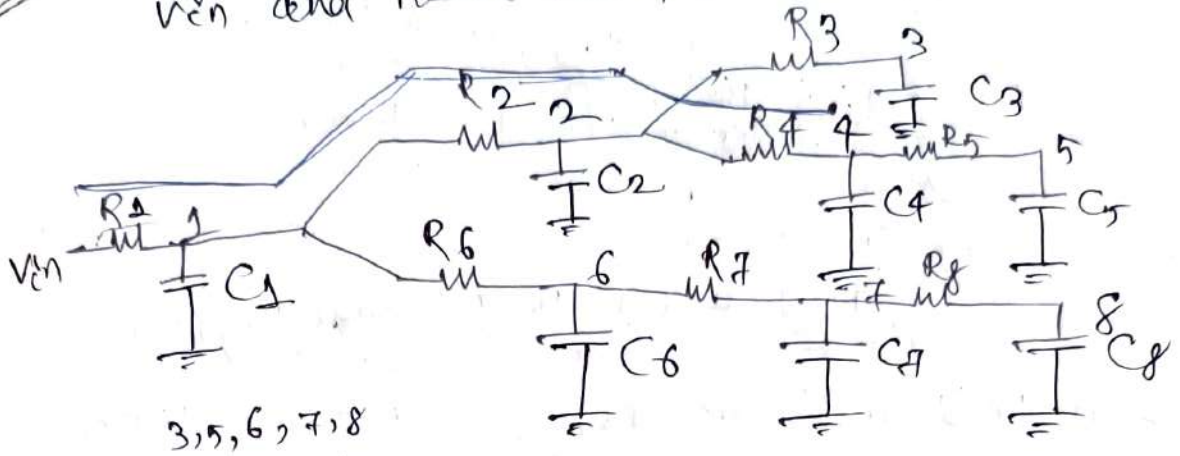
$R_1C_2 + R_1C_3 + R_1C_4 + R_1C_5$

Step-3 For the nodes coming under shortest path the delay is given by product of all previous resistances coming under shortest path & corresponding capacitance.

$R_1 C_1 + (R_1 + R_6) C_6 + (R_1 + R_6 + R_7) C_7$

$+ (R_1 + R_6 + R_7) C_8$.

Q. Find the delay between delay between vin and node no. 4.



3, 5, 6, 7, 8

$T_{D4} = R_1 C_1 + R_1 C_6 + R_1 C_7 + R_1 C_8$
$+ (R_1 + R_2) C_3 + (R_1 + R_2 + R_4) C_5 +$
$(R_1 + R_2) C_2 + (R_1 + R_2 + R_4) C_4$

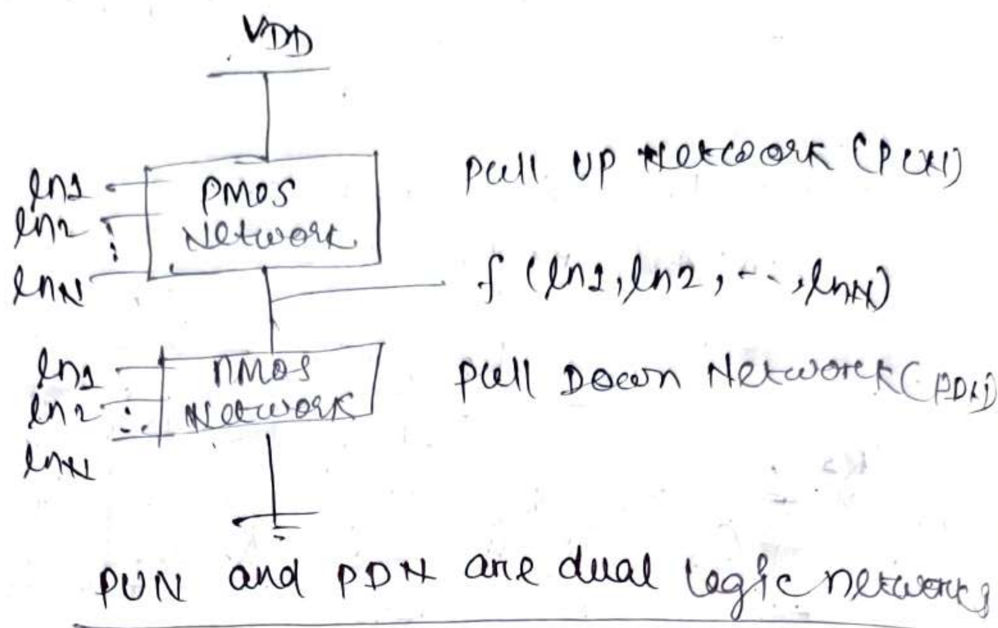
Module-2 Chapter-3

Combinational circuits :-

Static CMOS circuit :-

→ At every point in time (except during the switching transients) each gate output is connected to V_{DD} to V_{SS} via a low resistive path.

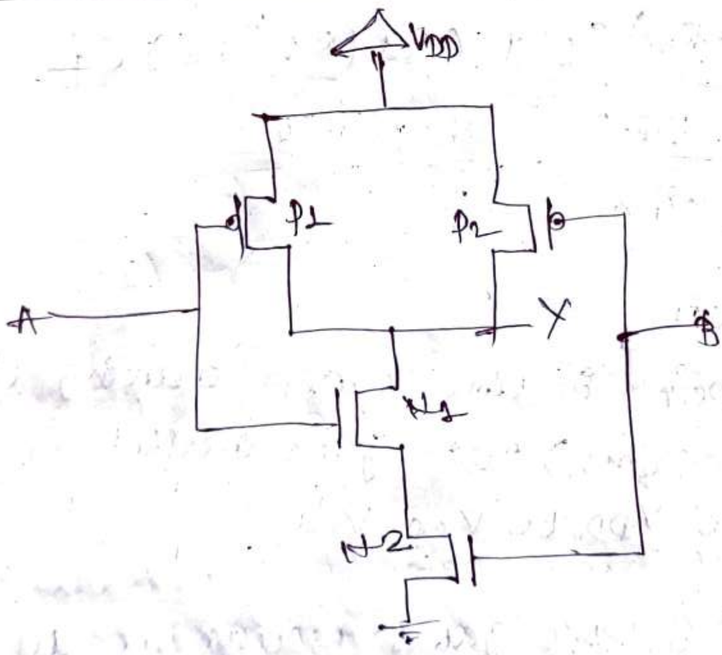
→ The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again,



PUN and PDN are dual logic networks

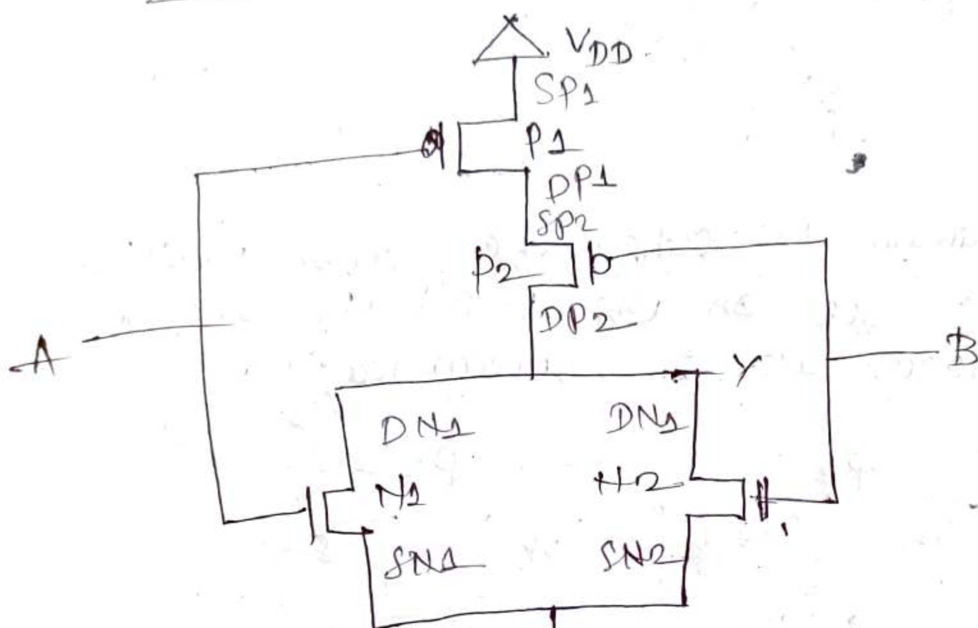
→ In this case, dual network means series combination of MOSFET will be replaced by parallel combination and vice-versa.

2-input NAND Gate :- (Transistor level)



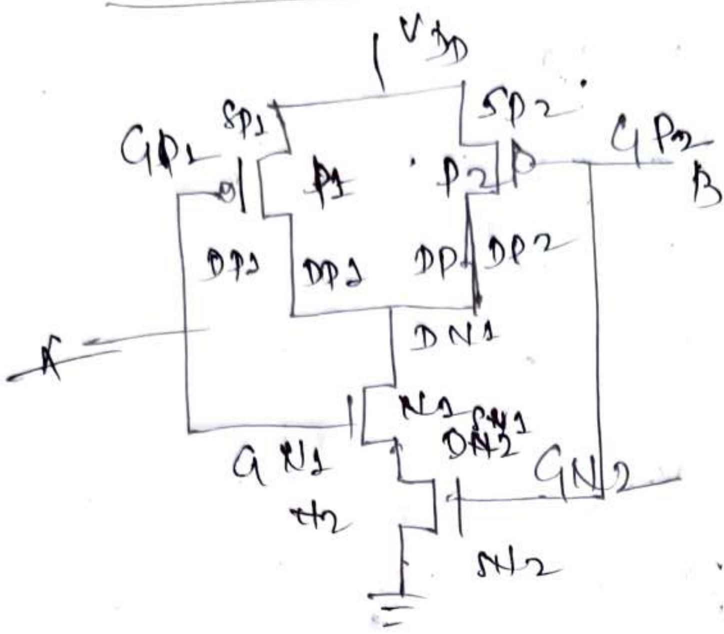
A	B	P_1	P_2	N_1	N_2	$Y = \overline{A \cdot B}$
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

2. Input NOR Gate :-

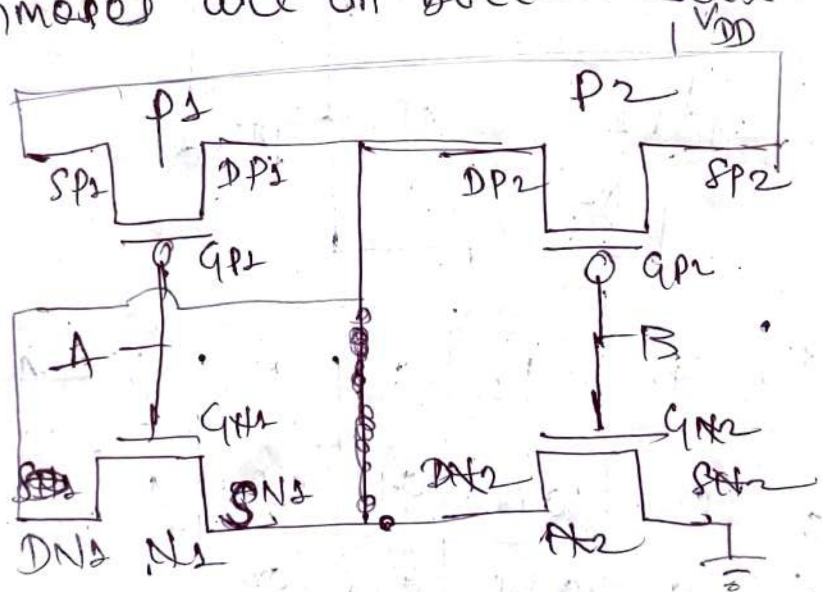


A	B	P_1	P_2	N_1	N_2	$Y = \overline{A + B}$
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

Layout of 2 input NAND gate:-

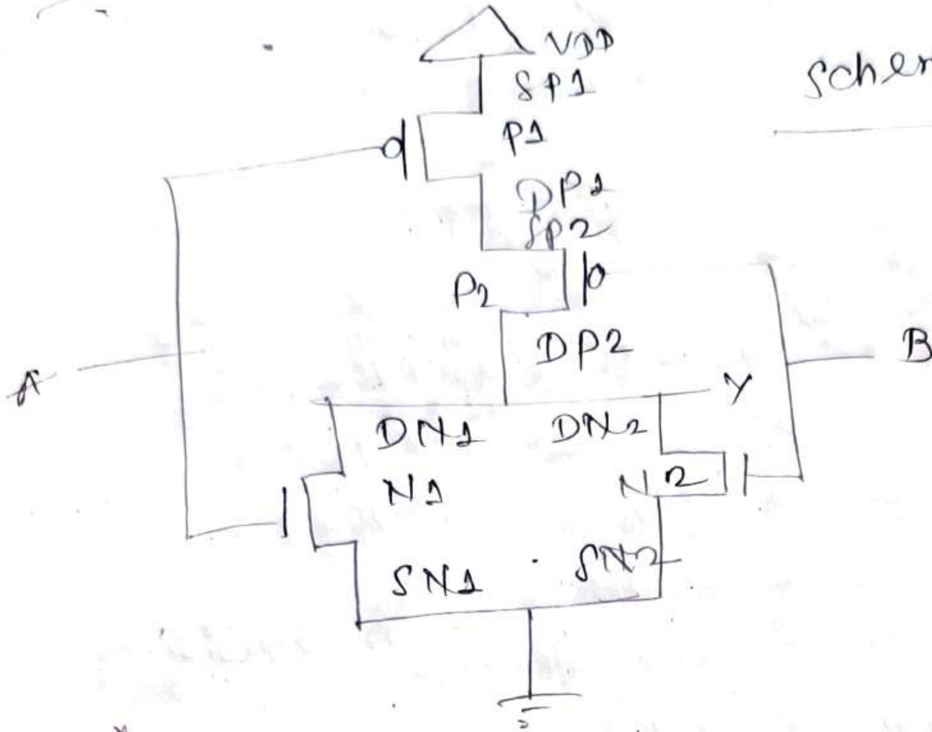


→ Re-draw the schematic such that all the pmos are on the top rail and all the nmoses are on bottom rail.

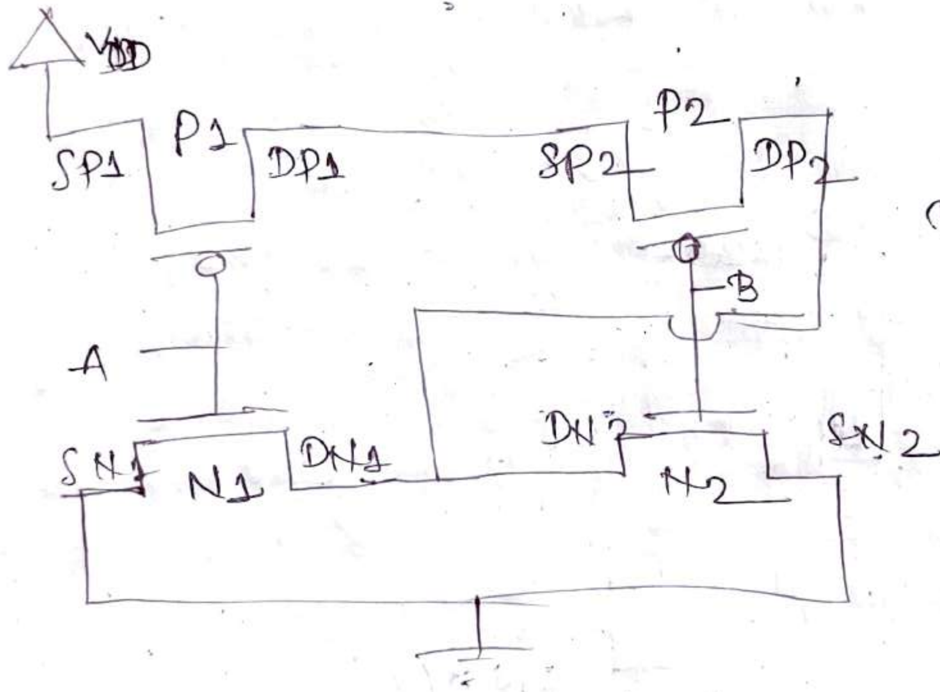


→ Connect the source, drain and connect the top pmos rail and bottom nmos rail such that least area is consumed.

Layout of NOR gate :-



Schematic diagram



Twisted diagram

Stick diagram :-

→ Does not contain any information of dimensions.

→ Represent relative positions of transistors.

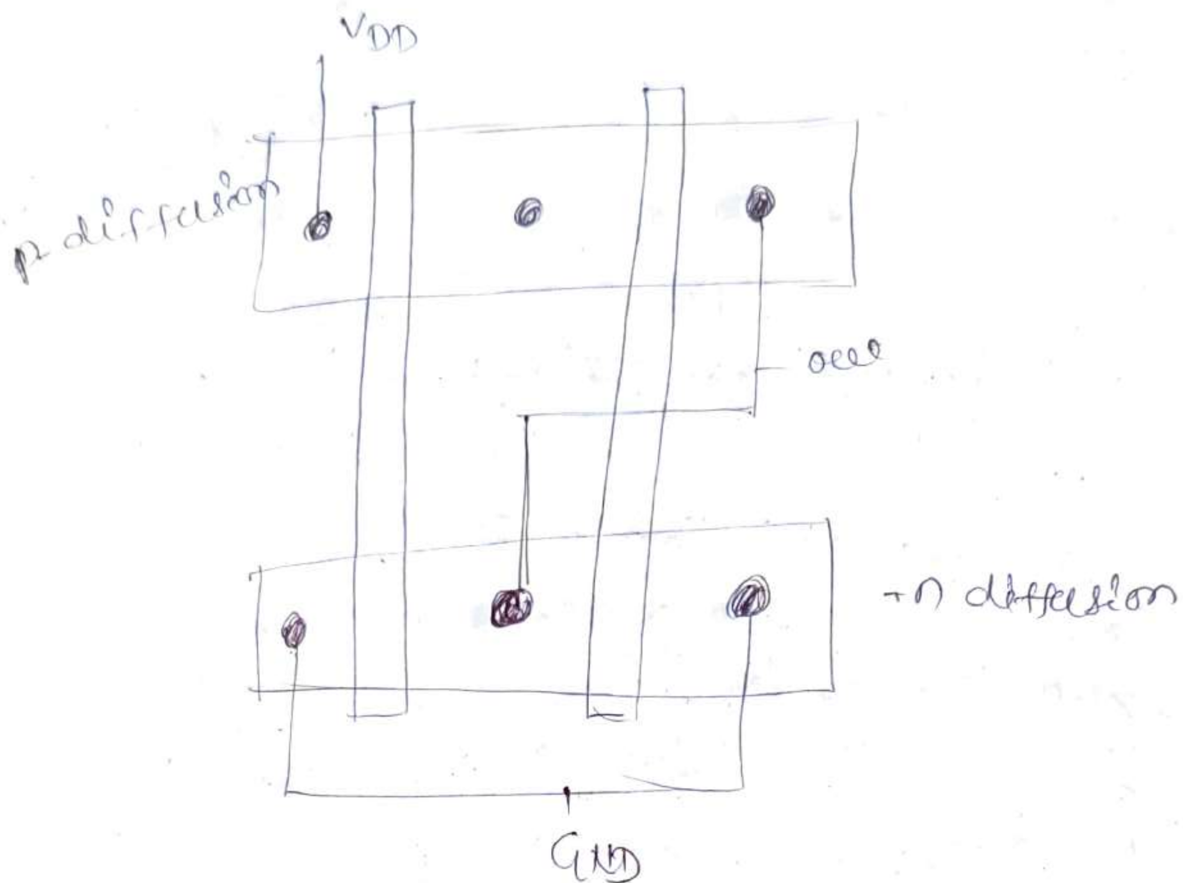
Basic elements :

→ Rectangle : Diffusion area.

→ solid line → metal connection

circle: contact

cross-hatched strip: polysilicon



Layout

VDD

Metal

Active contact

Active

p-diffusion

n well

Out/Y

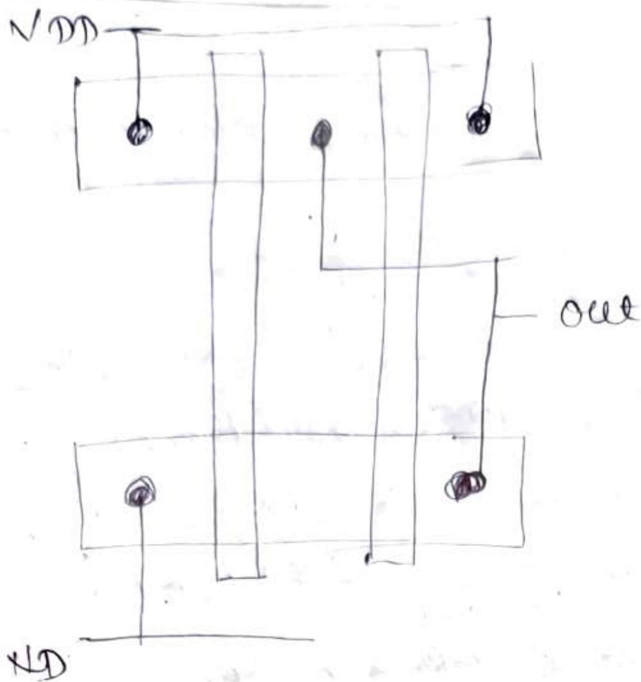
A

B

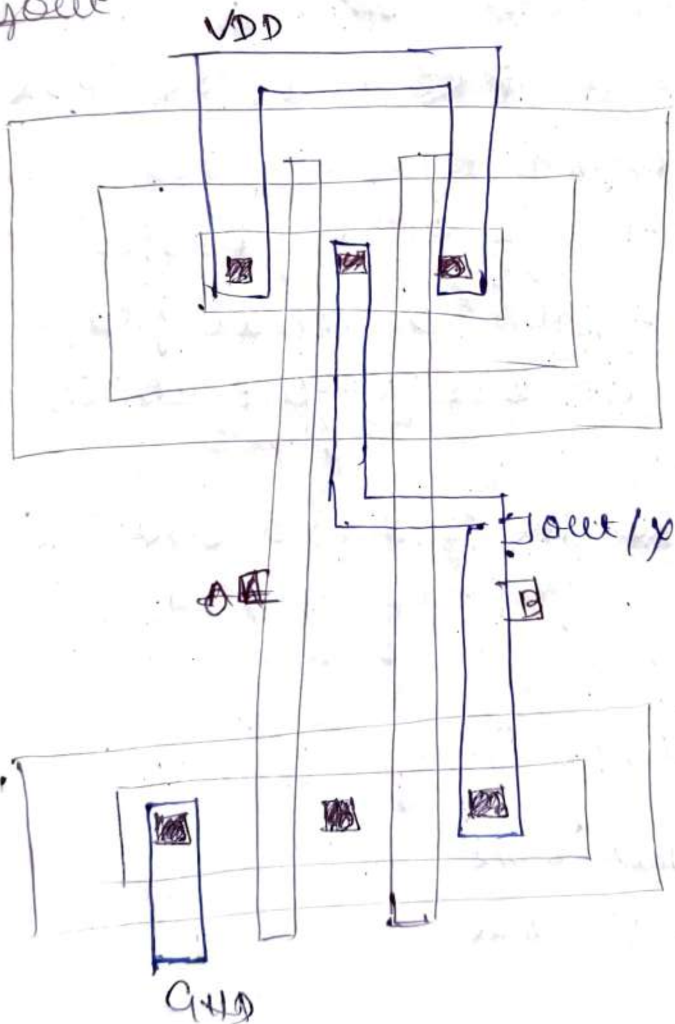
n-diffusion

Active

2 - i/p NAND Gate



Layout



Implementation of combinational logic functions using CMOS :-

→ Any CMOS circuit contains PDN and PUN.
(pull down n/w) (pull up n/w)

→ PDN :
- OR operations are performed by parallel-connected drivers.
- AND operations are performed by series connected drivers.
- Inversion is provided by the nature of MOS ckt operation.
- The PUN must be dual of PDN.
- Dual graph method is used to design the schematic of any boolean function.

→ Euler's path on dual graph network is used to find out layout consuming minimum area.

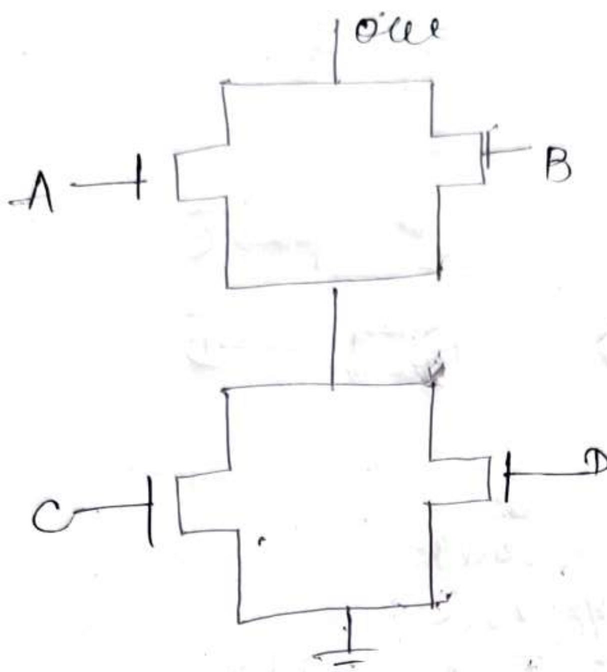
→ Let us take the following example to design the dual graph network and findout the corresponding layout.

eg. $Y = (A+B) \cdot (C+D)$

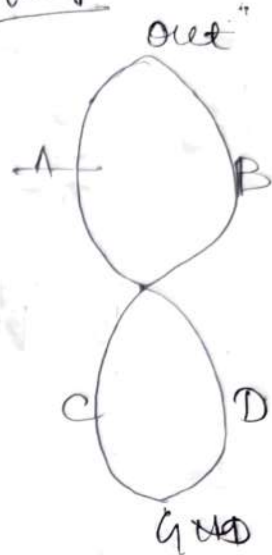
A - variable

A, $\bar{A}$ - literal

PDN

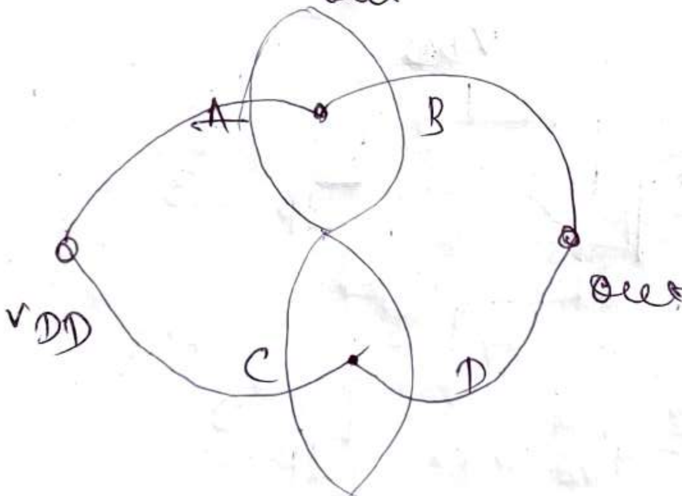


Graph

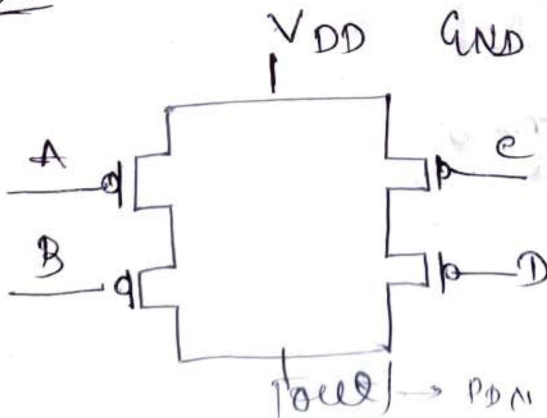


Steps to construct PUN from PDN :-

Step-1 Follow slide no. 21 from ppt.

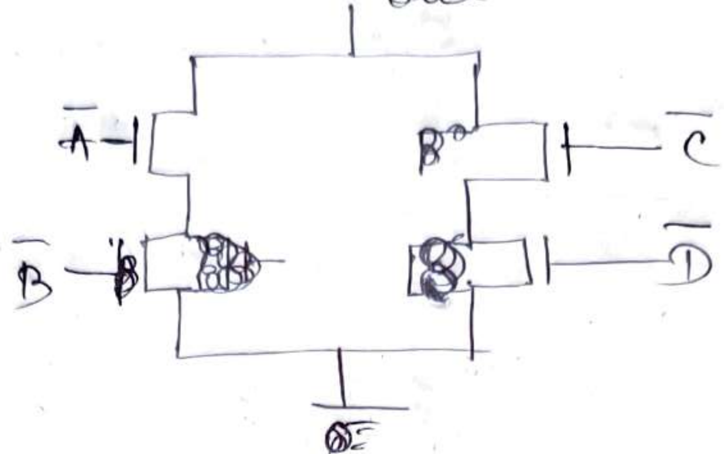


PUN

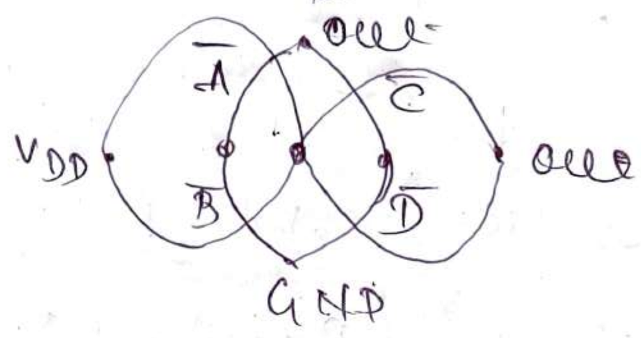


Q. $Y = \overline{(\bar{A} \cdot \bar{B}) + (\bar{C} \cdot \bar{D})}$

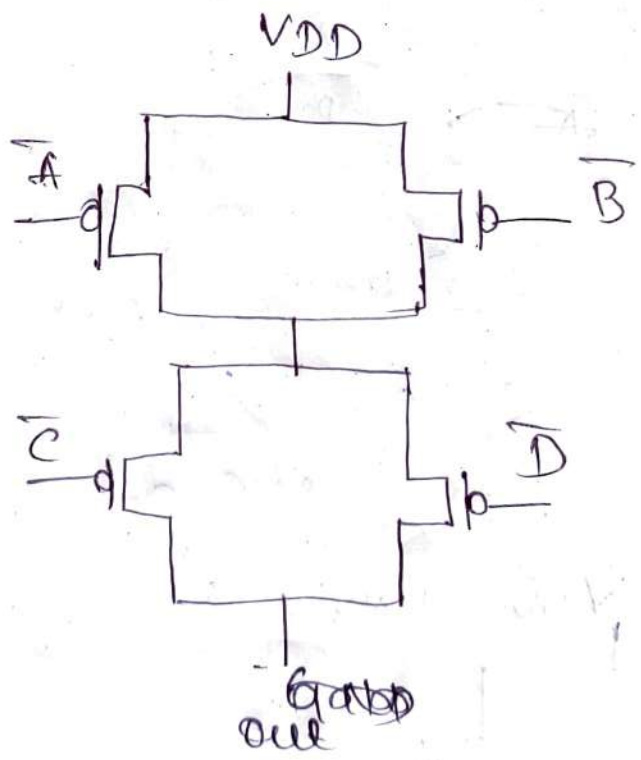
PDN

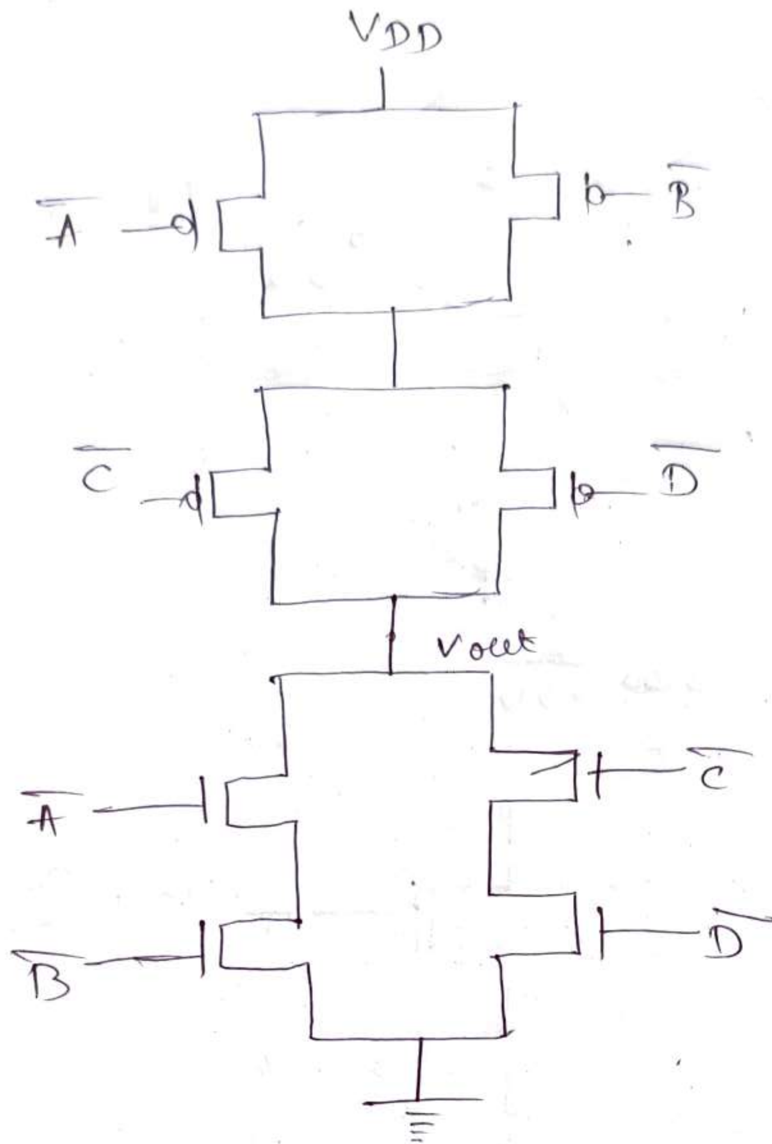


Graph



PUN

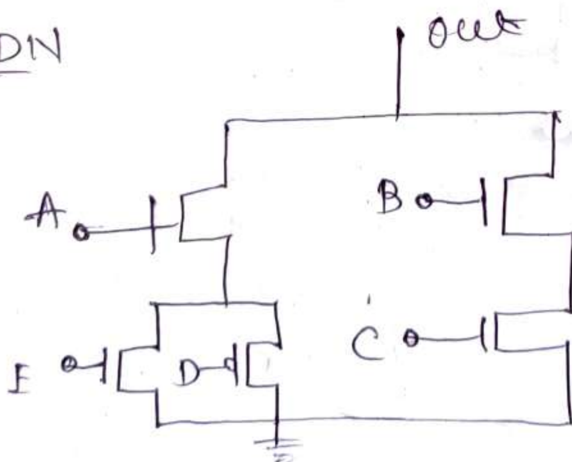




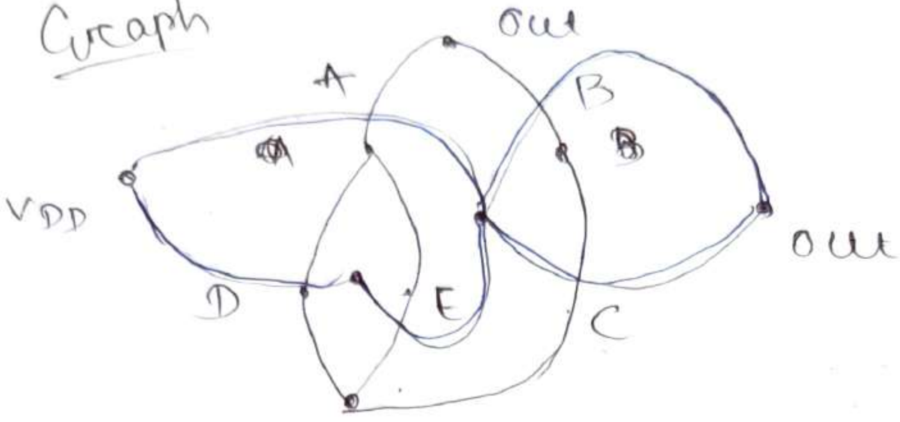
Q.

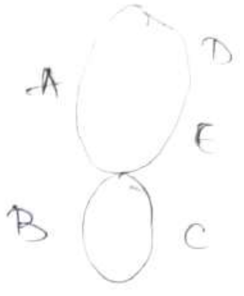
$$Y = \overline{(A \cdot (D+E)) + (B \cdot C)}$$

PDN

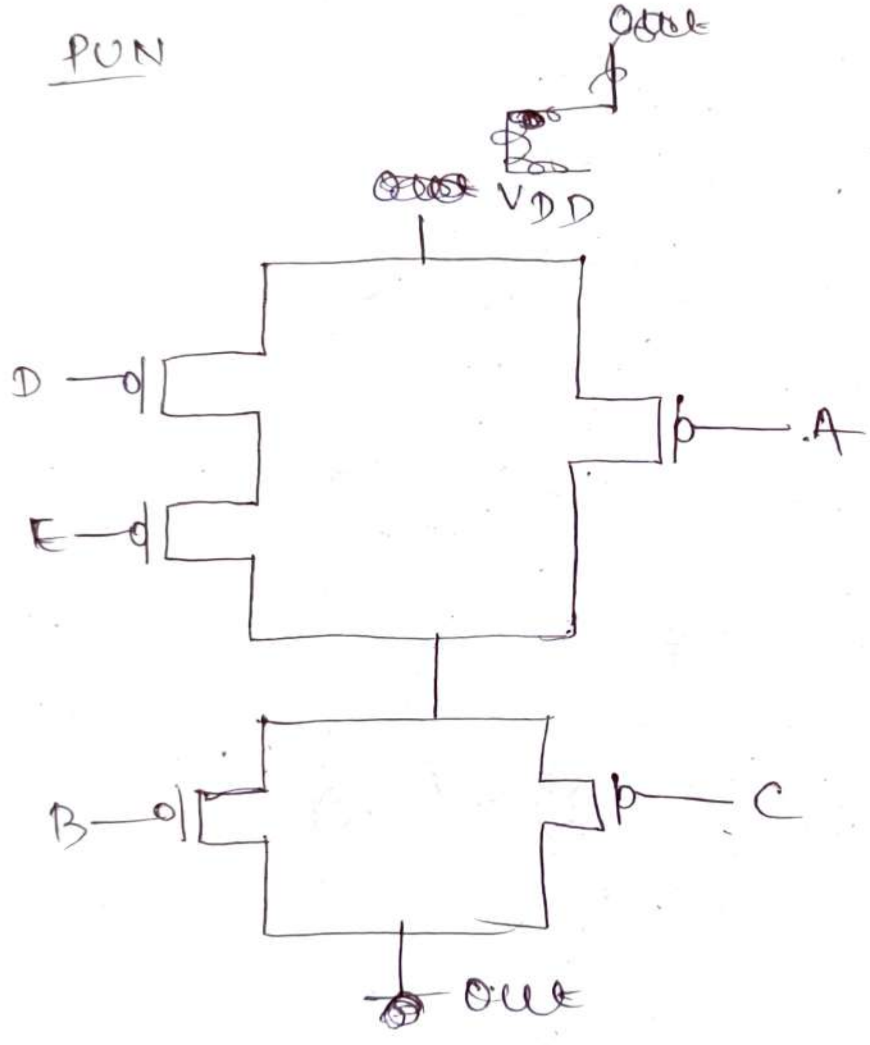


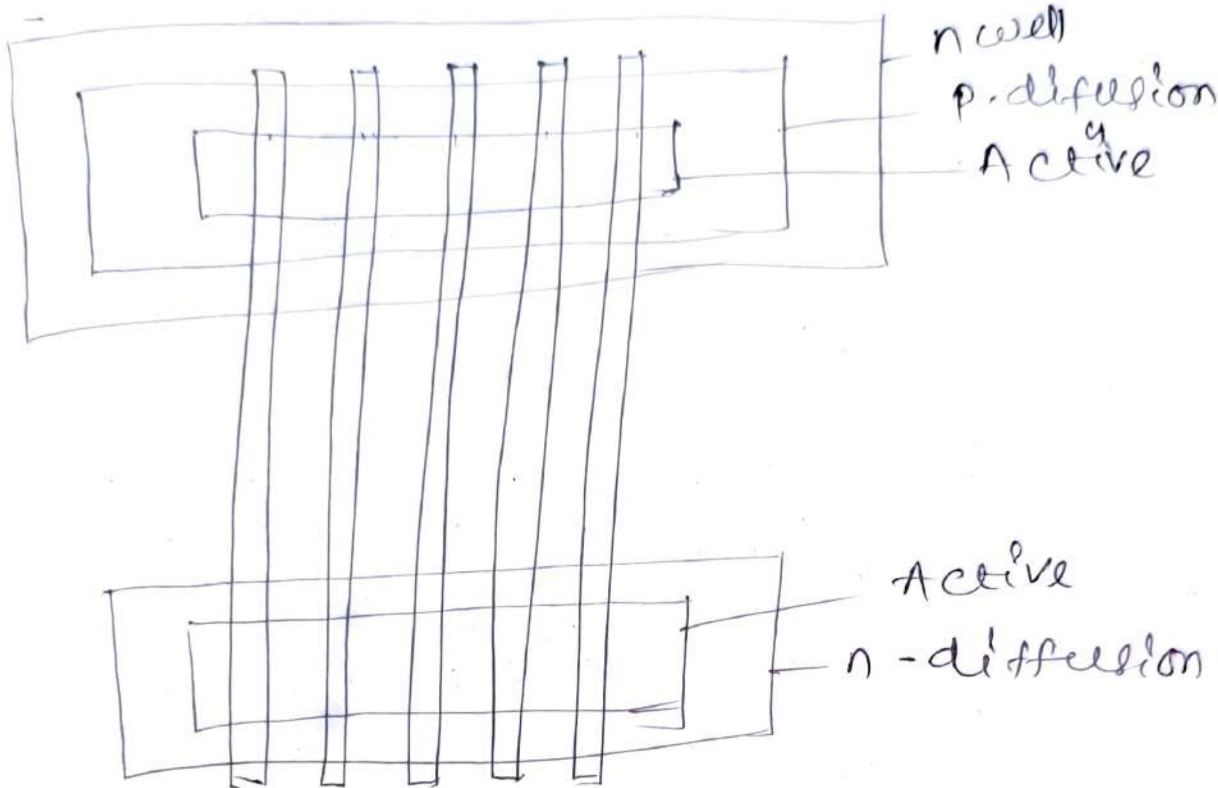
Graph





PUN




n well
p-diffusion
Active
Active
n-diffusion