EC - 705

B.E. VII Semester

Examination. December 2013

VLSI Design

Time : Three Hours Maximum Marks : 70

Note: Attempt only one question from each unit. Each question carries equal marks

UNIT – I

1. a) Explain the operation ofn-channel enhancement MOSFET with different values of Gate voltage.
b) What do you mean by hybrid technology? Describe the thick film and thin film circuits.

OR

2. a) Explain the following terms:-
i) Oxidation ii) Lithography iii) Ion-Implantation iv) Epitaxy
b) Discuss about the Bipolar process in detail.

UNIT – II

3. a) Draw and explain small-signal MOSFET model.
b) Explain short channel devices. Also mention its applications, advantages and limitations.

OR

4. a) Explain the dc model for(i) Diode (ii) BJT
b) Explain the method for measurement of λ and K.

UNIT-III

5. a) Explain the simulation of a circuit using SPICE with suitable flowchart.
b) Compare the high-frequency model of BJT and MOSSFET.

OR

6.a) Explain the level I large single MOSFET model.

b) Explain noise model for MOSFET as well as BJT.

UNIT-IV

a) Explain and differentiate the random logic forms and stridulated logic forms.
14 Describe the Bit-serial processing elements in details.

OR

8. a) Discuss the working of a static register cell.
b) What is Algotronix? Explain its architecture with detail.

UNIT- V

9. a) Discuss the steps of n-well CMOS fabrication process with suitable diagram.

b) Explain the following tarns w ith respect to latch up:
i) Physical origin
ii) Latch-up prevention

OR

10. a) Explain the basic steps for the fabrication process flow
b) What is the circuit elements? Describe the various type of circuit elements in detail.