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06CS33

Third Semester B.E. Degree Examination, June-July 2009
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Write the truth table of the logic circuit having 3 inputs A, B & C and the output expressed as $Y = A\bar{B}C + ABC$. Also simplify the expression using Boolean Algebra and implement the logic circuit using NAND gates. **(06 Marks)**

b. What is the purpose of using an expander with an AND – OR – INVERT gate? Write a logic circuit of an expander driving expandable AND – OR – INVERT gate. **(04 Marks)**

c. Simplify the following logic expression using Karnaugh map and also by Quine – McClusky method.

$$f(A, B, C, D) = \sum m(1, 2, 8, 9, 10, 12, 13, 14)$$ **(10 Marks)**

2 a. Write the truth table of a 4-bit Binary to Gray code converter and realize the same using four 74151 ICs (8-to-1 multiplexer) **(10 Marks)**

b. Realize 7-segment decoder using PLA. **(06 Marks)**

c. Write Verilog code for a combinational logic circuit that compares two 4-bit numbers A and B and generates a 3-bit output Y. The 3 bits of Y represent A = B, A > B and A < B. **(04 Marks)**

3 a. Show the 8-bit subtraction of these decimal numbers in 2's complement representation
i) +68, – 43 ii) +16, – 38 **(04 Marks)**

b. What is a fast adder? Show how two IC 74283s can be connected to add two 8-bit numbers. **(06 Marks)**

c. What is an ALU? How A < B function is performed in IC 74181? Also, show how 7 can be subtracted from 13 using IC 74181. **(10 Marks)**

4 a. Draw carefully the waveforms at points A, B and C in Fig.4(a). **(06 Marks)**

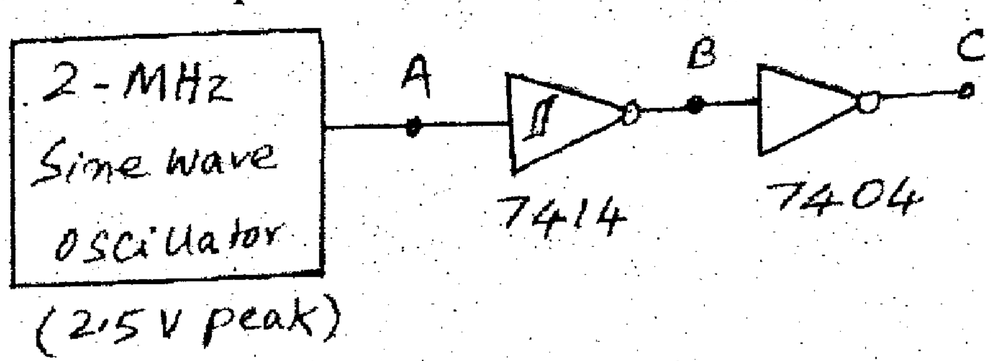

Fig.4(a)

b. Differentiate transparent and gated flip-flops. What are their applications? **(04 Marks)**

c. Show how to convert D flip-flop to JK flip-flop. **(10 Marks)**

PART – B

5 a. Name the four basic types of shift registers, and draw a block diagram for each. **(04 Marks)**

b. Draw the gates necessary to decode the 16 states of a mod-16 counter 7493. What are decoding glitches? How to eliminate them? **(10 Marks)**

c. What are presettable counters? What is lock out of a counter? Show how to construct a mod-13 counter using 74163 synchronous binary counter IC. **(06 Marks)**

6 a. Draw state transition diagram of a sequence detector circuit that detects '1101' from input data stream using both Mealy and Moore models. (1st Data bit = 1, 2nd data bit = 1, 3rd Data bit = 0 and 4th Data bit = 1). **(08 Marks)**

b. Design a parity generator using asynchronous sequential logic that gives output = 1 when it receives odd number of pulses and output = 0 if the number of pulses received is even. **(08 Marks)**

c. What are the problems with asynchronous sequential circuits? **(04 Marks)**

7 a. What is accuracy and resolution of the D/A converter? What is the resolution of a 12-bit D/A converter which uses a binary ladder? If the full-scale output is +10V, what is the resolution in volts? **(04 Marks)**

b. Find the following for a 12-bit counter-type A/D converter using a 1-MHz clock:
i) Maximum conversion time
ii) Average conversion time
iii) Maximum conversion rate **(06 Marks)**

c. Explain successive approximation A/D converter. **(10 Marks)**

8 a. Draw the circuit for a CMOS inverter and explain its working. **(06 Marks)**

b. Discuss the features of High-speed TTL, Low-power TTL and Schottky TTL families. **(06 Marks)**

c. Explain methods for interfacing CMOS devices to TTL devices. **(08 Marks)**

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