Code No. : 5307/M

FACULTY OF INFORMATICS
B.E. 4/4 (IT) II Semester (Main) Examination, May/June 2012
EMBEDDED SYSTEMS

Time: 3 Hours] [Max. Marks : 75

Note : *Answer **all** questions of Part **A**, Answer **any five** questions from Part **B**.*

PART – A **(25 Marks)**

1. Draw the various levels of abstraction in the embedded design process.
2. Distinguish between requirements and specifications.
3. Define interrupt vector table.
4. What are register banks in 8051 ?
5. List the interrupts in ARM and SHARC.
6. Define context switching.
7. What are message queues ?
8. What are the stages in instruction execution of 5-stage pipeline of ARM ?
9. Distinguish between serial and parallel communications.
10. What is instruction-level and cycle-level simulator ?

PART – B **(50 Marks)**

11. a) Explain the challenges to design embedded systems.
    b) Draw the block diagram of 8051 microcontroller with supporting hardware and explain.
12. a) Write an assembly language program to find whether a given number is positive or negative.
    b) What are the instruction types in 8051 ? Explain.

13. a) Explain pre-emptive and cooperative multitasking.
    b) Explain the interrupt routines handled procedure in RTOS.

14. a) Distinguish between Emulators and Simulators.
    b) Explain Hard real-time scheduling and soft real-time scheduling considerations.

15. a) Compare Von-newmann and Harvard architectures.
    b) Compare RISC and CISC.
    c) List all are the arithmetic and logical instructions in ARM.

16. a) What are the characteristics of Embedded processors ?
    b) Draw the architecture of Timers and explain.

17. Write short notes on :
    a) A/D and D/A converters.
    b) Instruction-level parallelism.
