

N.B. (1) Question No. 1 is compulsory.

(2) Attempt any four out of remaining six questions.

(3) Assume any suitable data wherever required but justify the same.

1. (a) For obtaining symmetrical characteristics comment on the aspect ratios of load and the driver. If the mobility ratio of electron to holes is 3:1. 20
 (b) CMOS NAND with CMOS NOR gate based on different parameters.
 (c) Butted and Buried contacts in VLSI
 (d) Skew rate in case of VLSI Design.
 (e) Define super-buffer and state the need of the same.

2. (a) Derive expression for drain current in nMOS device. 10
 For a nMOS device if —

$$\mu_n = 520 \text{ cm}^2 / \text{V} \cdot \text{sec} \quad t_{\text{ox}} = 12 \text{ nm}$$

$$\epsilon_{\text{ox}} = 3.9 \times 8.85 \times 10^{-14} \text{ F/cm} \quad W = 1.2 \mu\text{m} \quad L = 0.5 \mu\text{m}$$

$$V_G = -5 \text{ Volts} \quad V_{\text{THP}} = -1.5 \text{ Volts}$$

Find Drain current if $V_{\text{DS}} = -2 \text{ Volts}$.

State the condition in which the transistor is in and explain why ?

- (b) Find the expression for Threshold voltage of nMOS device also explain the effect of substrate potential (Body Effect) on Threshold. 10

Find the threshold shift due to body effect.

$$\text{Where } V_{\text{SB}} = 3 \text{ Volts} \quad N_A = 3 \times 10^{16} \text{ cm}^{-3} \quad t_{\text{ox}} = 300 \text{ \AA}$$

$$\epsilon_0 = 8.85 \times 10^{-14} \quad \epsilon_{\text{ox}} = 3.9 \epsilon_0 \quad \epsilon_{\text{si}} = 11.7 \epsilon_0$$

$$n_i = 1.5 \times 10^{10} \text{ cm}^{-3} \quad q = 1.6 \times 10^{-19} \text{ C}$$

3. (a) Compare enhancement and depletion type of loads used in nMOS Inverter circuit. Draw proper diagram. State clearly the different parameters which characterize each type of Inverters. 10
 (b) Explain in great detail the transfer characteristics of CMOS Inverter. Draw the transfer characteristics and explain all five regions clearly. 10

4. (a) $F = a + (b \cdot c \cdot d)$ 10

Consider the logical function as given above

(i) Design the CMOS logic gate that provides the function.

(ii) Is it possible to find an Euler graph for the circuit ? If so, construct the graph and also draw stick diagram and layout.

- (b) What is total power dissipation in case of CMOS Inverter ? Discuss how to approximate the estimation of total power dissipation ? Derive expression for short circuit power dissipation for CMOS Inverter. 10

5. (a) CMOS Inverter device is to be fabricated, describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. 10

- (b) What is sheet resistance ? 10

Find resistance R_n for nMOS if electron mobility $\mu_n = 560 \text{ cm}^2 / \text{V} \cdot \text{sec}$, $t_{\text{ox}} = 10 \text{ nm}$, $\epsilon_{\text{ox}} = 3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$, and $V_G = 3.3 \text{ Volts}$, $V_{\text{THP}} = 0.7 \text{ Volts}$ —

(i) if $W = 10 \mu\text{m}$ $L = 0.5 \mu\text{m}$

(ii) if channel width is increased to a value of $W = 22 \mu\text{m}$ while the Channel length remains same.

6. (a) What is pass transistor ? State advantages of transmission gate. Explain the method to design 8:1 MUX using nMOS. Also draw stick diagram for the same. 10
- (b) What is significance of scaling ? Its requirement and limitations. Explain various methods of scaling and compare them. 10
7. Write short notes on any **four** of the following :— 20
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|---------------------------------------|------------------------------|
| (a) Design Rules and its Significance | (d) Latch up Problem in CMOS |
| (b) Testability in case of VLSI | (e) Photolithography. |
| (c) Hot Electron Effect | |
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