2/6/2011
AGJ 1st half (x) 4

B E ETRX VIII (Rev)
Elective II - DSP Processors & Architectures

Con. 3983-11. (REVISED COURSE) RK-4635

(3 Hours) [Total Marks : 100

N.B. 1 Question No. 1 is compulsory.
2 Out of the remaining questions attempt any 4 questions.
3 All questions carry equal marks.

Q1

With respect to programmable digital signal processors in general, write a comprehensive note on the architectural features covering the points of bus and memory structure, MAC unit, pipelining feature, multi-ported memories etc. (20)

Q2

a) With a neat block diagram explain the architecture of TMS320C5X processor. Highlight the functions of central arithmetic logic unit (CALU) and auxiliary register ALU (ARAU). (14)
b) List the on-chip peripherals and their functions in TMS320C5X processor. (06)

Q3

a) With the help of examples explain the various addressing modes of C5X processor (14)
b) Explain briefly the addition and subtraction instructions in C5X processor. (06)

Q4

a) Explain the architectural features of ADSP 21xx series of digital signal processors. Compare the same with those of TMS320C5X series. (14)
b) How does the clock (crystal) speed affect the system through-put in a typical controller based system? What are the techniques used by designers to retain high through-put at lower crystal speeds for reducing EMI. (06)

Q5

a) Discuss the architectural features of TMS320C6X digital signal processor and compare the same with DSP563XX from Motorola. (14)
b) What is the need for high speed, high resolution ADC and DAC in digital signal processors along-with switched capacitor filters? (06)

Q6

a) Write a detailed note on the pipelining operation in C5X series of digital signal processors, with the help of illustrative instruction examples. (14)
b) List the on-chip peripherals and their functional requirements in C5X series of digital signal processors. (06)

Q7 Write short notes on: (20)
a) FFT algorithm using a typical DSP.
b) Implementation of FIR/IIR filters on a DSP.