Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 07

BCA (2009 to 2010 Batch) (Sem.–2)

DIGITAL CIRCUIT AND LOGIC DESIGN

Subject Code : BC-205

Paper ID : [B0209]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains SIX questions carrying TEN marks each and a student has to attempt any FOUR questions.**

SECTION-A

l. Write briefly :

(a) State De Morgan's theorem.

(b) Show that a Positive Logic NAND gate is negative Logic NOR gate.

(c) Differentiate Decoder from Demultiplexer.

(d) What is the drawback of SR Flip-Flop? How is it minimized?

(e) Differentiate between synchronous and asynchronous counters.

(f) What is Hamming code?

(g) What is Shift Register and give various type of registers.

(h) Express Gray code 10111 into binary number.

(i) What is Race around condition?

(j) Define Fan-in and Fan-out.

SECTION-B

2. Design a full adder and full subtractor.

3. Find a minimal SOP representation for

   f (A, B, C, D, E) = Σm (1, 4, 6, 10, 20, 22, 24, 26) + d (0, 11, 16, 27) using K-map method. Draw the circuit of minimal expression using only NAND.

4. Explain the working of Master Slave J-K flip flop and how the Race around condition can be removed by using Master Slave J-K flip flop?

5. An 8-bit byte with binary value 0101111 is to be encoded using an even parity Hamming code. What the binary vale after encoding?

6. Draw a block diagram for 4-bit bi-directional Shift Register with parallel load and explain its operation.

7. Design 2 bit count-down counter. (up-down counter)