SE | ETRX | III (REV) 19/5/2012

mk.H.1stHlf12.18

Basic Electronic Circuits

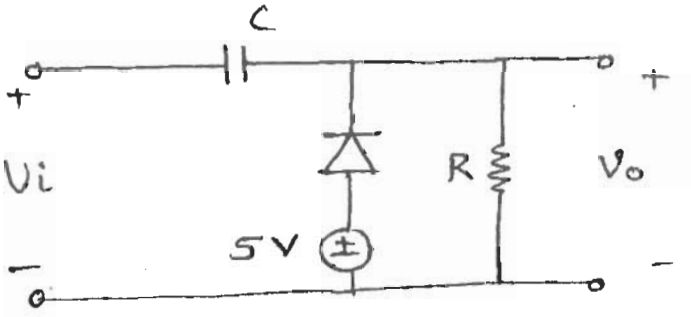
Con. 3760-12. GN-5282

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory** and solve any **four** questions out of remaining **six** questions.
(2) Assume **suitable** data if **necessary** and mention that assumption while solving that question.
(3) **Figures** to the **right** indicate **full** marks.

1. Any **four** :—

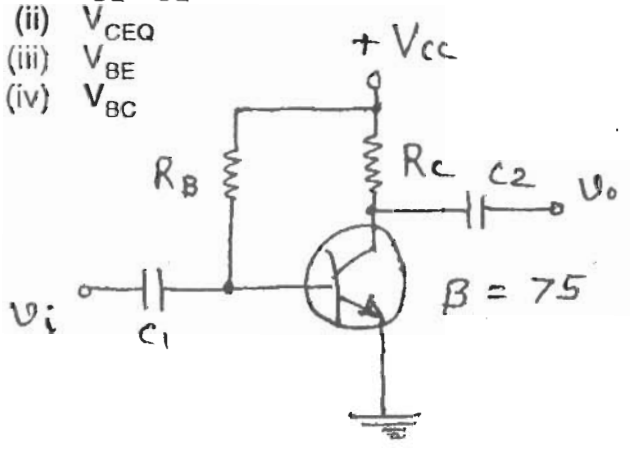
(a) If input V_i is 1 kHz square wave with 30 V p-p voltage applied to a given circuit with practical diode of silicon. Determine V_0 and draw waveform. 5



C = 1mF
R = 100 KW

(b) For the fixed-biased configuration given, determine the following :— 5

(i) I_{BQ}, I_{CQ}
(ii) V_{CEQ}
(iii) V_{BE}
(iv) V_{BC}



R_B = 240 kΩ
R_C = 2·2 kΩ
V_{CC} = +12 V
$C_1 = C_2$ = 10 μF

(c) Explain basic construction of a **n-channel** JFET and explain working of n-channel JFET for $V_{GS} = 0$ and $V_{GS} < 0$ and draw I_D v/s V_{DS} characteristic of the same. 5

(d) If I_E = 3·2 mA, h_{fe} = 150, h_{oe} = 25 μmho and h_{ob} = 0·5 μs for transistor then determine and draw : 5
(i) The common-emitter hybrid equivalent circuit
(ii) The common-base r_e model circuit.

(e) Compare 'L' and 'C' filter circuit. 5

2. (a) For a standard voltage-divider bias configuration of C-E amplifier with R_E bypassed by a capacitor CE the following data is given — 12

$V_{CC} = 22$ V, $R_1 = 56$ kΩ, $R_2 = 8{\cdot}2$ kΩ, $R_C = 6{\cdot}8$ kΩ, $R_E = 1{\cdot}5$ kΩ,

$C_{ci} = C_{co} = 10$ μF, $C_E = 20$ μF, $\beta = 90$.

Determine :

(a) r_e

(b) Z_i

(c) Z_0 for $r_0 = \infty\Omega$

(d) A_V for $r_0 = \infty\Omega$.

(e) Re-calculate parameters of part (b) through (d) if $r_0 = \frac{1}{h_{oe}} = 50\,k\Omega$ and compare the results.

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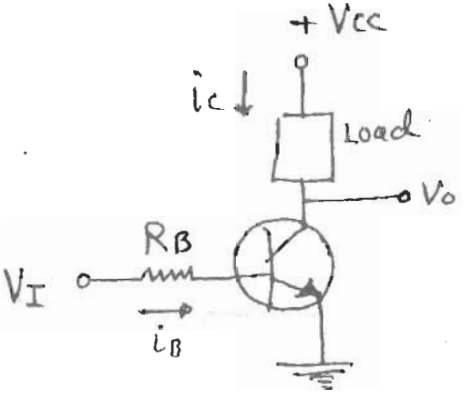
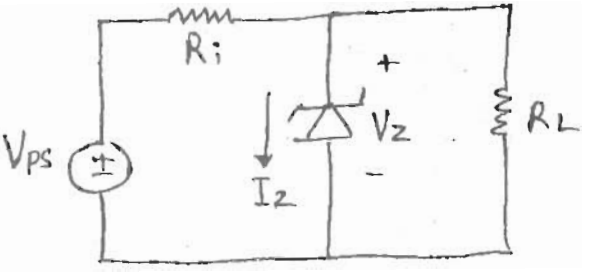
(b) A power transistor is used as a switch. Calculate the currents, output voltage and power dissipated in the transistor for the given circuit when $V_I = 0$ V and 12 V. Circuit and transistor parameters are : $R_B = 240\ \Omega$, $V_{CC} = 12$ V, $V_{BE\ (ON)} = 0{\cdot}7$ V, $V_{CE(Sat)} = 0{\cdot}1$ V, $\beta = 75$. Assume the load is a motor with an effective resistance of $R_C = 5\ \Omega$. 8



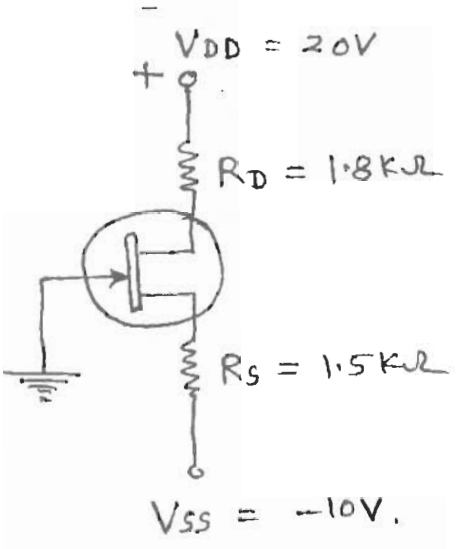
3. (a) Design a full wave bridge rectifier to meet particular specifications. It should produce a peak output voltage of 12 V and deliver 120 mA to the load R_L. Output must be with a ripple of not more than 5%. An input line voltage of 120 V (rms), 60 Hz is available. 8

(b) Draw and explain working of a voltage doubler circuit. 6

(c) The zener diode regulator circuit shown has an input voltage (V_{PS}) that varies between 10 and 14 V and load resistance varies between 20 Ω and 100 Ω. Assume 5·6 V. Zener diode is used and assume $I_{Z\ (min.)} = 0{\cdot}1\ I_{Z\ (max)}$. Find the value of R_i required and the minimum power rating of the diode. 6



4. (a) Determine the following for the given network I_{DSS} = 9 mA and V_P = –3 V. 10



(1) I_{DQ} and V_{GSQ}
(2) V_{DS}
(3) V_D
(4) V_S

You can use Graphical method.

(b) Draw npn BJT common collector (emitter follower) amplifier circuit and derive equation for small-signal voltage gain Av using rπ model. 10

5. Design a single stage CS JFET amplifier using potential divider biasing for the following specifications :— 20

   $V_0 = 2$ V
   $f_L = 20$ Hz
   $I_D = 3{\cdot}3 \pm 0{\cdot}6$ mA
   $|A_V| = 11$
   Use BFW 11.

   Calculate R_i, R_o and $V_{o\,(max)}$ for the designed amplifier.

6. Design a single stage CE BJT amplifier using BC 147A to satisfy the following specifications :— 20

   $|A_V| \geq 120$
   $SI_{CO} \leq 8$
   $V_{CC} = 24$ V
   $R_L = 10$ kW
   f_L is better than 10 Hz
   $I_{ca} = 3$ mA

   Estimate R_i and R_o of designed amplifier. If $R_i \geq 3$ KΩ is a new specification added then without changing the selected transistor suggest suitable modifications in the above design. What sacrifices you have made ?

7. Write short notes (any **three**) :— 20

   (a) Construction, working and transfer characteristic of n-channel enhancement type MOSFET
   (b) Comparison of performance of CE, CB and CC BJT amplifiers
   (c) Construction, process of electroluminescence of Light-Emitting Diode (LED)
   (d) Multistage Amplifiers
   (e) Photodiodes and Schottky Barrier Diode.

BEC DATA SHEET

nsistor type	Pdmax @ 25°C Watts	Icmax @ 25°C Amps	$V_{CE}^{(sat)}$ volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CER} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{BEO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal min.	typ.	h_{fe} max.	V_{BE} max.	θ_{fe} °C/W	Dera above 25°C W/°C
3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4
149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3
100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	0·05
47A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	220	260	0·9	—	—
525(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	—
47B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—

nsistor type	hie	hoe	hre	θja
147A	2·7 K Ω	18μ ℧	1·5 × 10^{-4}	0·4°C/mw
525 (PNP)	1·4 K Ω	25μ ℧	3·2 × 10^{-4}	—
147B	4·5 K Ω	30μ ℧	2 × 10^{-4}	0·4°C/mw
100	500 Ω	—	——	——
149	250 Ω	—	——	——
055	100 Ω	—	——	——
3055	25 Ω	—	——	——

BFW 11—JFET MUTUAL CHARACTERISTICS

–Vgs volts	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
Ids max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·5	0·0
Ids typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
Ids min. mA	4·0	3·0	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

Channel *JFET*

Type	V_{DS} max. Volts	V_{DG} max. Volts	V_{GS} max. Volts	P_d max. @25°C	T_j max.	I_{DSS}	g_{mo} (typical)	$-V_P$ Volts	r_d	Derate above 25°C	θ_{ja}
822	50	50	50	300 mW	175°C	2 mA	3000 μ ℧	6	50 KΩ	2 mW/°C	0·59°C/mW
V 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ ℧	2·5	50 KΩ	——	0·59° C/mW