33-1st Half-12 mina (e)

Con. 3999-12.   GN-7208

(3 Hours)   [Total Marks : 100

N. B. : (1) Question No. **1** is **compulsory**.
  (2) Out of remaining **six** questions, attempt any **four** questions.
  (3) In **all 5** questions to be **attempted**.
  (4) **Figures** to the **right** indicate **marks**.

1. (a) Enlist the instruction pairing rules of U and V pipeline in Pentium.   5
  (b) Write short note on Intel's Net burst micro architecture.   5
  (c) Draw the data flow graph for computation of integer power $Z = X^n$ of an   5
  input number X.
  (d) State the use of following x 86 flags :   5
      RF, TF, VM, NT, IOPL.

2. (a) Explain how the flushing of pipeline is minimized in Pentium architecture.   10
  (b) Explain in brief integer instruction pipeline stages of Pentium processor. List the   10
  steps in instruction issue algorithm.

3. (a) Differentiate between Pentium and Pentium pro-processors wrt size of address/data   10
  bus, addressable memory, virtual memory, L2 cache, generation, SMP support,
  integer pipeline stages, no. of integer pipes, floating point pipeline stages, no. of
  floating point pipes.
  (b) State the features of Intel Itanium processor. Draw the block diagram of Itanium   10
  processor and explain in brief.

4. (a) Explain segmentation and paging in protected mode of 80386 processor.   10
  (b) Explain the Debug registers of 80386DX processor.   10

5. (a) Consider the following reservation table for a unifunction pipeline :—

	0	1	2	3	4	5	6	7	8
S1	X								X
S2		X	X					X	
S3				X					
S4					X	X			
S5							X	X	

  (i) Find the forbidden set of latencies   2
  (ii) State the collision vector   1
  (iii) Draw the state transition diagram   5
  (iv) List simple cycles and greedy cycles   1
  (v) Calculate MAL (minimal average latency).   1
  (b) Explain static data flow computer architecture with example.   10

6. (a) Differentiate between real mode and protected mode of X 86 family. 10

   (b) Explain Cache organization of Pentium. 10

7. Write short note on the following :—

    (a) Structure of segment descriptor 5

    (b) USB 5

    (c) Layered architecture of SCSI 5

    (d) EISA. 5