M 22910

Reg. No. : .....

Name : .....

VIII Semester B.Tech. Degree (Reg./Sup. – Including Part Time) Examination, April 2013
(2007 Admn. Onwards)
PT2K6/2K6 EC 805(D) : EMBEDDED SYSTEMS

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Explain what is the distinction between specification and architecture. **5**
2. Compare and contrast top-down and bottom-up design. **5**
3. What is the difference between Harvard and Von Nueman architecture ? **5**
4. What data types does the SHARC support ? **5**
5. Draw and explain the CAN data frame format. **5**
6. Explain the Ethernet CSMA/CD algorithm. **5**
7. Write short notes on Round-robin scheduling. **5**
8. Explain priority driven scheduling. **5**

PART – B

1. a) What are the typical nonfunctional requriements of an embedded system ? **5**
   b) Explain what is architectural design by taking the example of a moving map. **10**

   OR

2. Draw a unified modeling language class diagram for the train controller showing the composition of the subsystems. Show how a set-inertia command flows through the refined class structure of the UML class diagram, moving from a change on the front panel to the required changes on the train.
   a) Show it in the form of a collaboration diagram.
   b) Show it in the form of a sequence diagram. **15**

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OR

4. a) Explain in detail the basic I/O devices commonly used in embedded system. **5**

   b) Explain the flow control in SHARC. **10**

5. Describe how an IP packet may be sent from a client on one ethernet to a client on a second ethernet. The two ethernets are connected by a router. **15**

OR

6. a) Explain what is distributed embedded architecture. Why would any one build a distributed embedded system ? **7**

   b) Explain the basic format of an IP packet. **8**

7. Explain in detail Earliest-Deadline-First scheduling. **15**

OR

8. Explain the following : **15**

   i) Blocking inter process communication.

   ii) Non-blocking inter process communication.
