C 26884 (Pages : 2) Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, MAY 2012

EE 09 405 / PT EE 09 404—DIGITAL ELECTRONICS

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

1. Define propagation delay in IC's.
2. Name any two IC packages.
3. Why are NAND and NOR called universal gates ?
4. Differentiate between level triggered and edge triggered FF.
5. What are flags ? What are their uses ?

(5 × 2 = 10 marks)

Part B

6. Draw the circuit of 2 input CMOS NAND gate. What are its advantages over TTL ?
7. What are open-collector o/ps ? Also state the function of pull up resistor ?
8. Explain priority—encoders.
9. Define ROM, PROM, EPROM, EEPROM and CDROM.
10. Construct a Full adder in PROM, PAL and PLA.
11. What are microinstructions ? Explain with example.

(4 × 5 = 20 marks)

Part C

12. (a) Draw the circuit schematic of TTL inverter and CMOS inverter. Compare the characteristic of each family.

Or

(b) Explain mixed voltage interfacing concept with relevant diagram.

13. (a) (i) With an example, explain the use of Karnaugh map for reducing 5 variable expressions. (7 marks)

(ii) Differentiate between Decoder and Demultiplexer. (3 marks)

Or

(b) Design and draw the circuit of Binary to BCD code converter

Turn over

14. (a) Using state reduction techniques, design a synchronous circuit to detect a sequence of 3 consecutive 1's occurring in a series.

Or

(b) Explain the circuit of DRAM and also discuss the read and write operations with timing diagram.

15. (a) Discuss the ALU.

Or

(b) List the various addressing modes of 8085 microprocessor and write a program to find the maximum number in an array.

(4 × 10 = 40 marks)