M.E. sem II (Rev.) Etrx Microprocessor & System II 02/12/08.

Con. 5417–08. (REVISED COURSE) BB–8333

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining questions.
(3) State any additional data assumed, if **necessary** to answer.

1. (a) Explain the conditions under which the Pentium performs 'burst cycles' and only with timing diagram, explain the burst cycle from main memory to processor. **12**
   (b) Explain with a neat diagram, Pentium state transitions. **8**

2. (a) Explain the "Write Once" policy as implemented in the Pentium Processor with examples, assuming that Lz Cache is present. **10**
   (b) Explain the functional Redundancy Check feature of the Pentium. **10**

3. (a) Explain the need and working of the Branch Prediction Logic. Explain clearly the structure of the BTB. **10**
   (b) Explain the interrupt subsystem of the Pentium in detail. **10**

4. (a) Explain the process of data transfer over the PCI Bus with following reference :– **15**
      (i) Bus mastering and its latency
      (ii) Data Phases
      (iii) Priorities for bus masters.
   (b) Write a detailed note on special cycle of the Pentium processor. **5**

5. (a) Explain the function of the following PCI Bus signals – **10**
      (i) $\overline{\text{DEVSEL}}$
      (ii) $\overline{\text{FRAME}}$
      (iii) SDONE
      (iv) PAR
      (v) $\overline{\text{SBO}}$
   (b) What is meant by Bus Access Latency with reference to the PCI Bus. Also explain the function of the Latency timer. **10**

6. (a) Explain the basic features of a real time operating system (eg. QNX). **12**
   (b) Explain the importance of "interrupt handler" in the QNX operating system. **8**

7. (a) Compare the USB and Rs-232C interspace and justify the choice in terms of speed and addvisability for data transfers. **12**
   (b) Explain the process of USB device enumeration of any USB device of your choice. **8**
