8/05/13 BE (ETRx) Rev VIII Advance VLSI Design

55 : 1st half.13-shilpa(h)

Con. 7493-13. **(REVISED COURSE)** **GS-2965**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data wherever required and justify the **same**.

1. (a) Analog circuits design is difficult as compared to Digital circuit design. Justify. **5**
(b) Explain electromigration effect in an Inter connect. **5**
(c) Draw and explain trench capacitor and stacked capacitor structure of DRAM cell. **5**
(d) Write verilog code for 8-bit counter. **5**

2. (a) Draw the circuit using propagate and generate term for 4-bit CLA network, in **each** of the following :– **10**
(i) nFET logic
(ii) Pseudo nMos logic.
(b) Give and explain the capacitances associated with an interconnect and explain how propagation of signal depends upon the distributed RC effect. **10**

3. (a) The storage capacitor in a DRAM has a value of C_S = 55 fF. The circuitary restricts the capacitor voltage to a value of V_{max} = 3·5 V; When the access transistor is off, the leakage current of the cell is estimated to be 75 nA. **10**
(i) How many electrons can be stored on C_S ?
(ii) How many fundamental charge unit q leave the cell in 1 second due to leakage current ?
(b) Give various important parameter affecting switching performance of C MOS Inverter. Suggest methods to improve it. **10**

4. (a) Give and explain maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. **10**
(b) Implement following functions using AND-OR PLA :– **10**

$X = ac + \overline{b}c$

$Y = abc + \overline{a}\overline{b}c$

$Z = \overline{a}b + ab$

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5. (a) Give and explain Interconnect scaling with its width, length, thickness and capacitances. **10**

   (b) Give and explain single phase clock system and explain its drowback. **10**

6. (a) Draw and explain C MOS two stage OP-AMP. Give gain boosting technique. **10**

   (b) Draw and explain Schmitt - trigger circuit as a input protection for C MOS. Also explain bi-directional I/O circuits. **10**

7. Write short notes on (any **three**) :– **20**

   (a) Frequency compensation scheme of CMOS Amplifier

   (b) Manchaster carry chain circuits and MODL Circuit

   (c) Pipelined system

   (d) EEP ROM Programming technique.

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